

# nPZero power-saving IC Datasheet

## Overview

The nPZero is a power-saving IC that enables ultra-low power autonomous operation in sensor-based systems, eliminating the need for an always-on MCU. It takes over the role of system controller by powering down the MCU, controlling I<sup>2</sup>C/SPI communication buses, and autonomously managing up to four connected sensors. When a trigger condition is met, such as a threshold-crossing sensor value or external interrupt, the nPZero can power up the MCU, handing back system control.

## Key Specifications

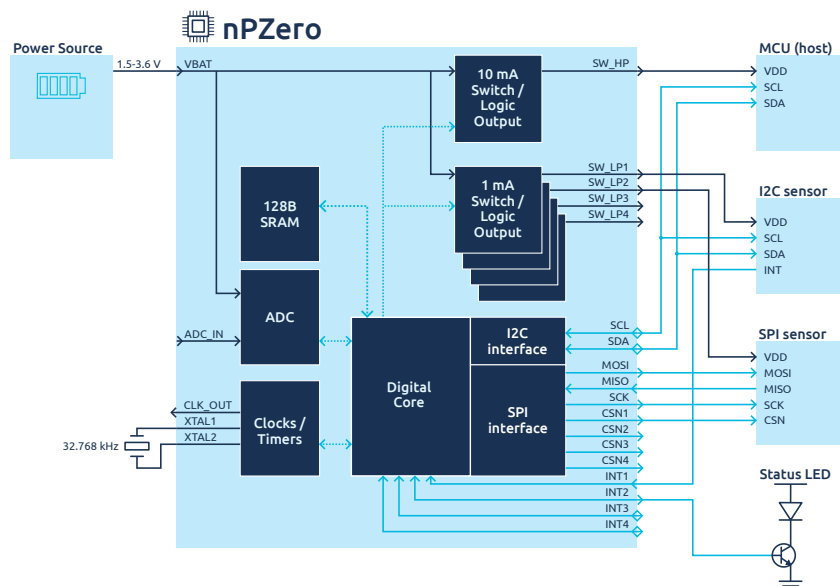
- **Supply voltage:** 1.5 - 3.6 V
- **Idle current:** 100 nA
- **Polling current:** 1.0  $\mu$ A
- **Host switch max current:** 10 mA
- **Sensor switch max current (x4):** 1 mA
- **I<sup>2</sup>C / SPI frequency:** 100 kHz
- **Package options:**  
QFN32, 5 $\times$ 5 mm; WLCSP34, 2.45 $\times$ 2.45 mm
- **Temperature range:** -20 $^{\circ}$ C to +85 $^{\circ}$ C

## Typical Applications

- Battery-powered or energy-harvesting-powered IoT devices
- Smart Buildings/Cities/Agriculture
- Tracking, Logging, Monitoring ++

## Features

- **Ultra-low-power standalone operation**
  - Power-cycling:  
turns off MCU and sensors when it is not needed
- **Autonomous operation of up to 4 sensors**
  - MCU is powered off
  - Polling of sensors with threshold-based wake-up triggers
  - Communication over I<sup>2</sup>C or SPI
  - Flexible I/O pins for interrupt inputs or trigger outputs
- **Supports one I<sup>2</sup>C MCU**
  - Configuration via I<sup>2</sup>C commands
  - nPZero IC wakes the MCU when required
- **Integrated power switches for the MCU and 4 sensors**
  - Can be changed to logic output to control external switches for higher currents
- **128-byte SRAM**
  - Initialization commands for the sensors
  - General purpose data
- **Optional crystal oscillator**
  - Improved timing accuracy
  - Programmable clock output
  - External 32.768 kHz crystal for higher precision timing



## Revision History

Revision	Date	Description
1.00	2024.11.21	Initial release
1.10	2025.07.02	<ul style="list-style-type: none"> <li>• Updated digital I/O characteristics;</li> <li>• Updated electrical characteristics;</li> <li>• Fixed TWT_E*_P[1-4] and TINIT_E*_P[1-4] register fields description;</li> <li>• Removed power switches automatic gate boost feature;</li> <li>• Sections and images updated;</li> <li>• Legal notices section added;</li> <li>• One-page summary added;</li> <li>• New document format applied</li> </ul>
1.20	2025.08.07	Information on the 28-pin package removed
<b>New revision numbering system adapted</b>		
0.93	2025.11.21	<ul style="list-style-type: none"> <li>• One-page summary rearranged, made as a title page;</li> <li>• Information on WLCSP34 package added;</li> <li>• Several pin names updated;</li> <li>• Default pin states table added;</li> <li>• DC characteristics table updated;</li> <li>• Current consumption at different operational cases table added;</li> <li>• Operation states terminology updated;</li> <li>• Typical application schematic and corresponding components table updated;</li> <li>• Typical performance section added;</li> <li>• REACH, ROHS subsection added;</li> <li>• New revision numbering system adapted</li> </ul>
0.94	2025.12.19	<ul style="list-style-type: none"> <li>• WLCSP34 pin package name corrected;</li> <li>• Typical application diagram and corresponding external components table updated;</li> <li>• Trigger area of threshold-compare-modes table updated</li> </ul>

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# 1 Overview

## 1.1 Introduction

The nPZero G1 (from now on referred to as nPZero or device) is a power-saving IC that can greatly reduce the power consumption of battery-constrained sensor applications. It accomplishes this by handling communication with sensors directly without requiring the involvement of an MCU (host) and supplying power to sensors only when they are needed using 4 individual power switches. A separate power switch allows control of a host MCU which will be shut off completely in normal operation but can be woken up based on a set of configurable wake-up triggers.

Data readings from any of the connected sensors can be used as a trigger if the value is outside or inside a pre-defined range. Additionally, an ADC input allows analog signals to be used as a wake-up source. A low-power timer is used to allow for regular wake-up of the host in the absence of other wake-up triggers. An internal crystal oscillator is available if precise timekeeping is needed, and a dedicated clock output pin can be enabled to provide an accurate clock signal to other parts of the system.

An internal SRAM block is used for storing sensor initialization sequences and can also be used by the host for general data storage.

This document covers the nPZero G1 with part numbers listed in Table 1, it outlines expected specifications and is subject to change without further notification, e.g., following testing and characterization.

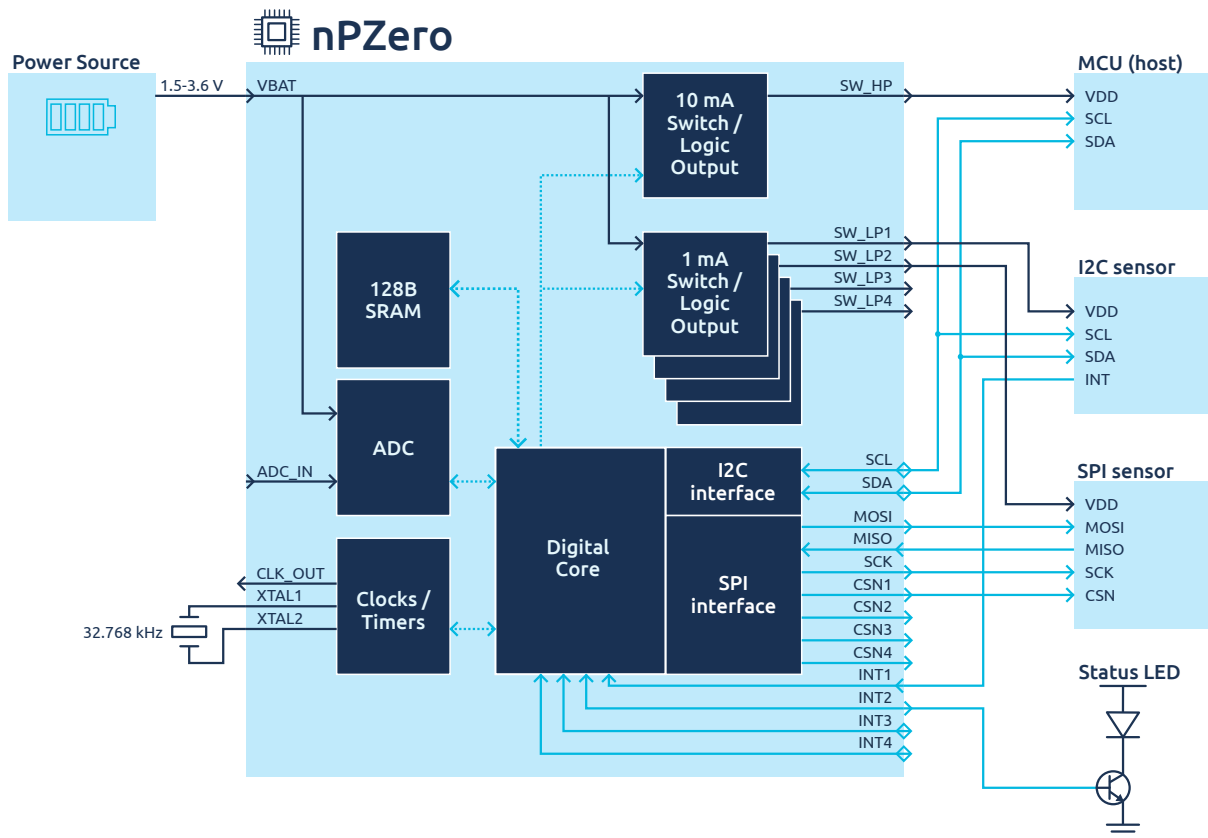


Figure 1: Illustration of the nPZero G1 in a system

## 1.2 Key Features

- **Low-power standalone operation**
  - Polling current consumption at 3.0 V: 1.0  $\mu$ A
  - Idle current consumption at 3.0 V: 100 nA
- **Autonomous operation of up to 4 independent peripherals**
  - Polling of sensors with threshold-based wake-up triggers
  - I<sup>2</sup>C or SPI serial protocols for communication
  - Flexible I/O pins can be used as interrupt inputs or trigger outputs
- **Supports one I<sup>2</sup>C host MCU**
  - Configuration via I<sup>2</sup>C commands
  - nPZero G1 wakes host when required
- **Integrated power switches for host and 4 peripherals**
  - 1 $\times$ 10 mA high-side switch for host
  - 4 $\times$ 1 mA high-side switches for peripherals
  - Can be changed to logic output to control external switches for higher current requirements
- **128-byte SRAM**
  - For initialization commands for the peripherals
  - For general purpose data
- **2-channel ADC**
  - 5-bit ADC for battery monitoring
  - 6-bit ADC for external input
- **Optional crystal oscillator (XO)**
  - Programmable clock output
  - External 32.768kHz crystal for higher precision system timekeeping
- **Supply voltage from 1.5 V to 3.6 V**
- **Operates from -20°C to +85°C**
- **QFN 32-pin package, 5 $\times$ 5 mm; WLCSP 34-pin package, 2.45 $\times$ 2.45 mm**

### 1.3 Variants

The datasheet covers the variants of the nPZero G1 listed below. Initial samples are available in QFN32 packaging variant. For more information on WLCSP options please contact the company via the website [www.nanopowersemi.com](http://www.nanopowersemi.com).

Table 1: Product number of variants covered by the datasheet

Product number
NPZG1S-Q32

### 1.4 Pin Description

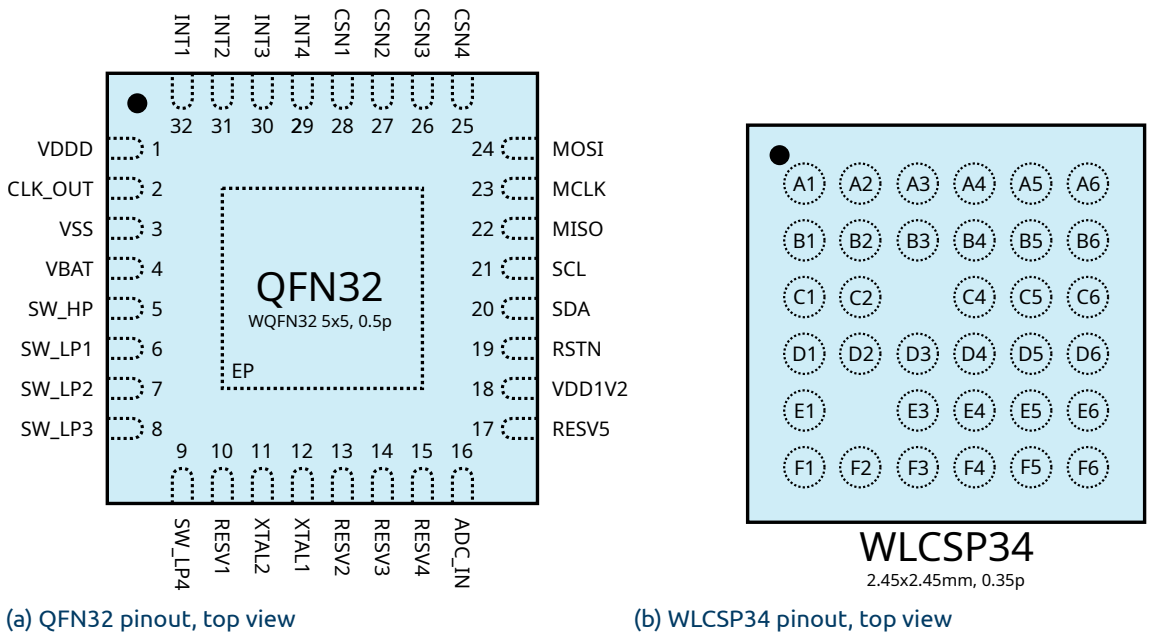


Figure 2: nPZero G1 pinout

Table 2: nPZero G1 pin description

QFN32	WLCSP34	Name	Type	Description
1	A6	VDDD	Analog	0.5V internal supply, bypass capacitor required
2	C5	CLK_OUT	Output	Programmable clock output derived from crystal oscillator
3	B6, C4, C2, E3	VSS	Power	Common ground
4	C6	VBAT	Power	Device supply voltage
5	D6	SW_HP	Output/ Power	Host device power output or logic output Set as power output (enabled) on reset
6	D5	SW_LP1	Output/ Power	Peripheral 1 power output or logic output Set as power output (disabled) on reset
7	E6	SW_LP2	Output/ Power	Peripheral 2 power output or logic output Set as power output (disabled) on reset
8	E5	SW_LP3	Output/ Power	Peripheral 3 power output or logic output. Set as power output (disabled) on reset
9	F6	SW_LP4	Output/ Power	Peripheral 4 power output or logic output Set as power output (disabled) on reset
10	D4	RESV1	–	Reserved, do not connect
11	F5	XTAL2	–	Crystal oscillator pin 2. Not connected, floating
12	F4	XTAL1	–	Crystal oscillator pin 1. Not connected, floating
13	E4	RESV2	–	Reserved, do not connect
14	–	RESV3	–	Reserved, do not connect
15	D3	RESV4	–	Reserved, do not connect
16	F3	ADC_IN	Analog Input	ADC external input
17	D2	RESV5	–	Reserved, do not connect
18	F2	VDD1V2	Analog	1.2V internal supply, bypass capacitor required
19	F1	RSTN	Input	Device reset, active low. Fixed internal pull-up ( $\approx 100k\Omega$ )
20	D1	SDA	I/O	I <sup>2</sup> C data. Internal pull-up enabled on reset ( $\approx 40k\Omega$ )
21	E1	SCL	I/O	I <sup>2</sup> C clock. Internal pull-up enabled on reset ( $\approx 40k\Omega$ )
22	C1	MISO	Input	SPI Master In Slave Out
23	B1	MCLK	Output	SPI serial clock output. Can be set to HiZ when not used or in Idle state
24	A1	MOSI	Output	SPI Master Out Slave In. Can be set to HiZ when not used or in Idle state
25	A2	CSN4	Output	Chip select (active low) for peripheral 4. Can be set to HiZ when not used or in Idle state
26	B2	CSN3	Output	Chip select (active low) for peripheral 3. Can be set to HiZ when not used or in Idle state
27	A3	CSN2	Output	Chip select (active low) for peripheral 2. Can be set to HiZ when not used or in Idle state
28	B3	CSN1	Output	Chip select (active low) for peripheral 1. Can be set to HiZ when not used or in Idle state

Table 2: nPZero G1 pin description

QFN32	WLCSP34	Name	Type	Description
29	A4	INT4	I/O	Peripheral 4 interrupt input or trigger output. Set to input w/ internal pull-up on reset ( $\approx 100k\Omega$ )
30	B4	INT3	I/O	Peripheral 3 interrupt input or trigger output. Set to input w/ internal pull-up on reset ( $\approx 100k\Omega$ )
31	A5	INT2	I/O	Peripheral 2 interrupt input or trigger output. Set to input w/ internal pull-up on reset ( $\approx 100k\Omega$ )
32	B5	INT1	I/O	Peripheral 1 interrupt input or trigger output. Set to input w/ internal pull-up on reset ( $\approx 100k\Omega$ )
EP	–	EP	–	Exposed pad. Connect to VSS

Table 3: nPZero G1 default pin states

Pins	Direction	If not used	Default State		
			Reset	Standby	Idle
CLK_OUT	Output	Do not connect	Undefined	Low	Low
SW_HP	Output	Do not connect	Undefined	Vbat	HiZ
SW_LP[1-4]	Output	Do not connect	Undefined	HiZ	HiZ
RESV1	–	Do not connect	Internal pull-up	Internal pull-up	Internal pull-up
XTAL2	–	Do not connect	HiZ	HiZ	HiZ
XTAL1	–	Do not connect	HiZ	HiZ	HiZ
RESV2	–	Do not connect	Internal pull-up	Internal pull-up	Internal pull-up
RESV3	–	Do not connect	HiZ	HiZ	HiZ
RESV4	–	Do not connect	HiZ	HiZ	HiZ
ADC_IN	Input	Do not connect	HiZ	HiZ	HiZ
RESV5	–	Do not connect	Internal pull-down	Internal pull-down	Internal pull-down
RSTN	Input	Do not connect	Internal pull-up	Internal pull-up	Internal pull-up
SDA	I/O	–	Undefined	Internal pull-up	HiZ
SCL	I/O	–	Undefined	Internal pull-up	HiZ
MISO	Input	Do not connect	HiZ	HiZ	HiZ
MCLK	Output	Do not connect	Undefined	HiZ	HiZ
MOSI	Output	Do not connect	Undefined	HiZ	HiZ
CSN[1-4]	Output	Do not connect	Undefined	HiZ	HiZ
INT[1-4]	I/O	Do not connect	Undefined	Internal pull-up	Internal pull-up

## 1.5 High-level Block Diagram

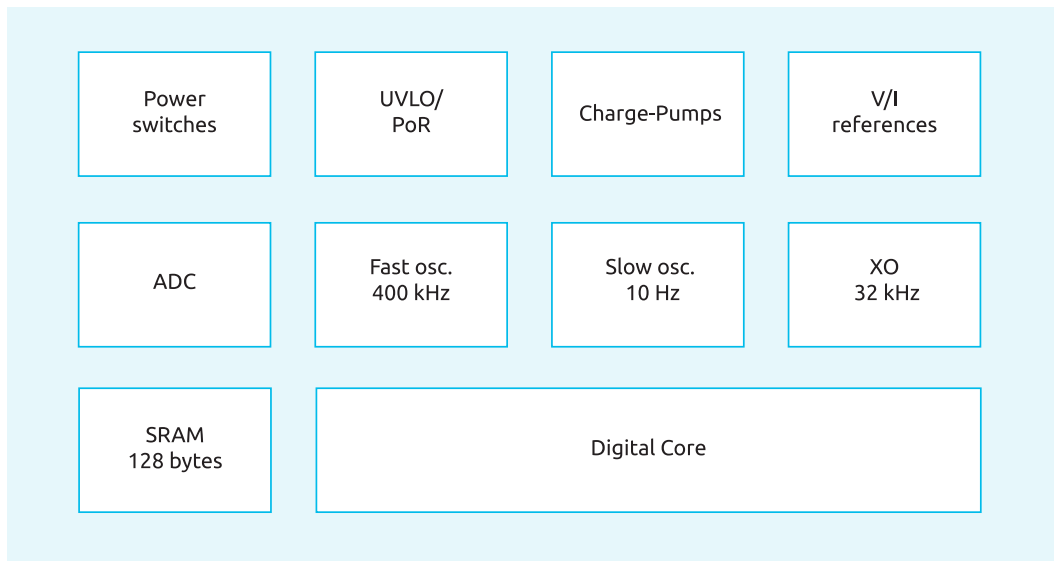


Figure 3: nPZero G1 high-level block diagram

## 1.6 Operating Conditions

Table 4: nPZero G1 operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>BAT</sub>	Supply voltage	1.5	–	3.6	V
T	Temperature range	-20	–	85	°C

## 1.7 Absolute Maximum Ratings

Exposure to operating conditions beyond the maximum ratings listed may cause permanent damage to the IC. These are maximum stress ratings and do not imply functional operation of the device at these or any other conditions beyond those in this section. Exposure to absolute-maximum-rated conditions for extended periods may affect the device's reliability. Absolute maximum ratings for V<sub>BAT</sub>, V<sub>DDD</sub>, V<sub>DD1V2</sub>, XTAL<sub>1</sub> and XTAL<sub>2</sub> pins are stated in Table 5 nPZero absolute maximum ratings, all other pins have same absolute maximum ratings as V<sub>BAT</sub> pin.

Table 5: nPZero absolute maximum ratings.

Symbol	Description	Min	Max	Unit
V <sub>BAT</sub>	Supply voltage pin	-0.3	3.9	V
V <sub>DDD</sub>	0.5V Internal supply pin	-0.3	2.16	V
V <sub>DD1V2</sub>	1.2V Internal supply pin	-0.3	2.16	V
XTAL <sub>1</sub>	Crystal oscillator pin 1	-0.3	2.16	V
XTAL <sub>2</sub>	Crystal oscillator pin 2	-0.3	2.16	V
T <sub>J</sub>	Operating junction temperature	-40	125	°C
I <sub>I/O</sub>	DC current per I/O pin	–	5	mA
V <sub>ESDCDM</sub>	ESD voltage using charged-device model (CDM)*,†	-500	500	V

\*Stress voltage to measure device susceptibility to damage caused by electrostatic discharge events.

†Level listed is the passing level per ANSI/ESDA/JEDEC JS-002.

## 1.8 Electrical Characteristics

Electrical specifications in this document are derived from our latest models and simulations. Specifications will be updated and expanded based on the physical samples' actual performance in future document revisions. Typical behaviour of nPZero IC including current consumption across different supply voltages and temperature conditions is provided in section 4 Typical performance.

### 1.8.1 DC Characteristics

DC characteristics are, unless otherwise stated, for typical conditions of  $T = 22^{\circ}\text{C}$  and  $V_{\text{BAT}} = 3.0\text{ V}$ .

Table 6: nPZero G1 DC characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_{\text{startup}}$	Startup time	–	150	–	ms
$V_{\text{BATSR}}$	$V_{\text{BAT}}$ slew rate	–	–	0.5	V/s
$V_{\text{BATESR}}$	$V_{\text{BAT}}$ series resistance	–	–	1.5	k $\Omega$
$V_{\text{ADC\_IN}}$	Analog input (ADC_IN) voltage range	0.6	–	$V_{\text{BAT}}$	V
$I_{\text{VBAT(RST)}}$	Current consumption during reset <sup>‡</sup>	–	–	50	$\mu\text{A}$
$I_{\text{LOAD(PSWH)}}$	Current load host PSW	–	–	10	mA
$I_{\text{LOAD(PSWP)}}$	Current load peripheral PSW	–	–	1	mA
$R_{\text{DS(on)(PSWH)}}$	On resistance host PSW	–	6	11	$\Omega$
$R_{\text{DS(on)(PSWP)}}$	On resistance peripheral PSW	–	35	75	$\Omega$
$V_{\text{PSWSR(on)}}$	PSW slew rate turning on	–	1 – 1.8	–	V/mS
$I_{\text{OLEAK}}$	Leakage current at output pins	–	–	1.5	nA
$T_{\text{RST}}$	RSTN pulse width to guarantee a reset	250	–	–	$\mu\text{s}$

<sup>‡</sup>nPZero G1 internal pull-up driven current.

## 1.9 Current consumption

Detailed information on current consumption at different operational cases is provided in Table 7.

Table 7: nPZero G1 current consumption at different operational cases

Symbol	Parameter	Operation state *	VCC	Typ	Max	Unit
I <sub>LFRC</sub>	Idle with @10Hz low-power oscillator	Idle	3.0V	100		nA
I <sub>LFRC,ADC</sub>	Idle with @10Hz low-power oscillator and ADC sampling @10Hz		3.0V	100		nA
I <sub>LFXO</sub>	Idle with XO @16Hz		3.0V	200		nA
I <sub>LFXO,ADC</sub>	Idle with XO @16Hz and ADC sampling @1024Hz		3.0V	350	500	nA
I <sub>LFXO,CO</sub>	Idle with XO @16Hz and clock out @32768Hz		3.0V	1.2 <sup>†,‡</sup>		μA
I <sub>HF,POLL</sub>	Polling mode	Polling	3.0V	1		μA
I <sub>HF,POLL,I2C</sub>	Polling mode during I2C communication		3.0V	1		μA
I <sub>HF,POLL,SPI</sub>	Polling mode during SPI communication		3.0V	1		μA
I <sub>HF,STANDBY</sub>	Standby mode	Standby	3.0V	1		μA
I <sub>HF,STANDBY,I2C</sub>	Standby mode during I2C communication		3.0V	1		μA

\*Operation states are explained in subsection 2.2

<sup>†</sup>for an external load capacitance of 20 pF

<sup>‡</sup>depends on an external load capacitance:  $I_{LFXO\_CO} \approx I_{LFXO} + C_{load} \times F_{CLK\_OUT} \times \frac{V_{BAT}}{2}$

### 1.9.1 Digital I/O characteristics

Table 8: nPZero G1 digital I/O characteristics

Symbol	Parameter	Min	Max	Unit
V <sub>IH</sub>	Digital input high voltage	0.8 × V <sub>BAT</sub>	V <sub>BAT</sub>	V
V <sub>IL</sub>	Digital input low voltage	0	0.2 × V <sub>BAT</sub>	V
V <sub>OH</sub>	High level output voltage	0.8 × V <sub>BAT</sub>	–	V
V <sub>OL</sub>	Low level output voltage	–	0.2 × V <sub>BAT</sub>	V

Table 9: nPZero G1 Output currents

Symbol	Parameter	Conditions	Pins	V <sub>BAT</sub>	Normal Strength	High Strength	Unit
I <sub>OH</sub>	High level output current	V <sub>OH</sub> =0.8 × V <sub>BAT</sub>	CLK_OUT MCLK MOSI CSN[1-4] SW_HP SW_LP[1-4] INT[1-4]	1.5 V	0.26	0.44	mA
				1.8 V	0.40	0.65	mA
				2.7 V	0.84	1.30	mA
				3.6 V	1.30	1.80	mA
I <sub>OL</sub>	Low level output current	V <sub>OL</sub> =0.2 × V <sub>BAT</sub>	CLK_OUT MCLK MOSI CSN[1-4] SW_HP SW_LP[1-4] INT[1-4]	1.5 V	0.41	0.64	mA
				1.8 V	0.58	0.88	mA
				2.7 V	1.10	1.50	mA
				3.6 V	1.60	2.10	mA
			SDA SCL	1.5 V	1.10	–	mA
				1.8 V	1.40	–	mA
				2.7 V	2.20	–	mA
				3.6 V	2.90	–	mA

### 1.9.2 Serial Communication Characteristics

Table 10: nPZero G1 Serial Communication Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
f <sub>SCL(S)</sub>	I <sup>2</sup> C slave SCL input frequency	–	–	–	100	kHz
f <sub>SCL(M)</sub>	I <sup>2</sup> C master SCL output frequency	–	–	100	–	kHz
f <sub>MCLK</sub>	SPI master MCLK output frequency	–	–	100	–	kHz

### 1.10 Typical Application

In a typical application, the nPZero G1 will control both the power supply of the host and both the power supply and the communication with the connected peripherals and host. This means the nPZero G1 can take over the controller role from the host, saving considerable power in periods when the host capabilities, e.g., wireless transmission or computing power, are not needed. The host will need to spend less time in active mode, and the sleep current of the host can be lowered significantly. At the same time, the nPZero G1 can reduce peripheral power consumption by powering them off when not in use, rendering peripheral sleep or standalone power consumption irrelevant.

Figure 4 shows a typical application diagram and required components when the nPZero G1 IC is used with two connected peripherals, one I<sup>2</sup>C sensor, and one SPI sensor.

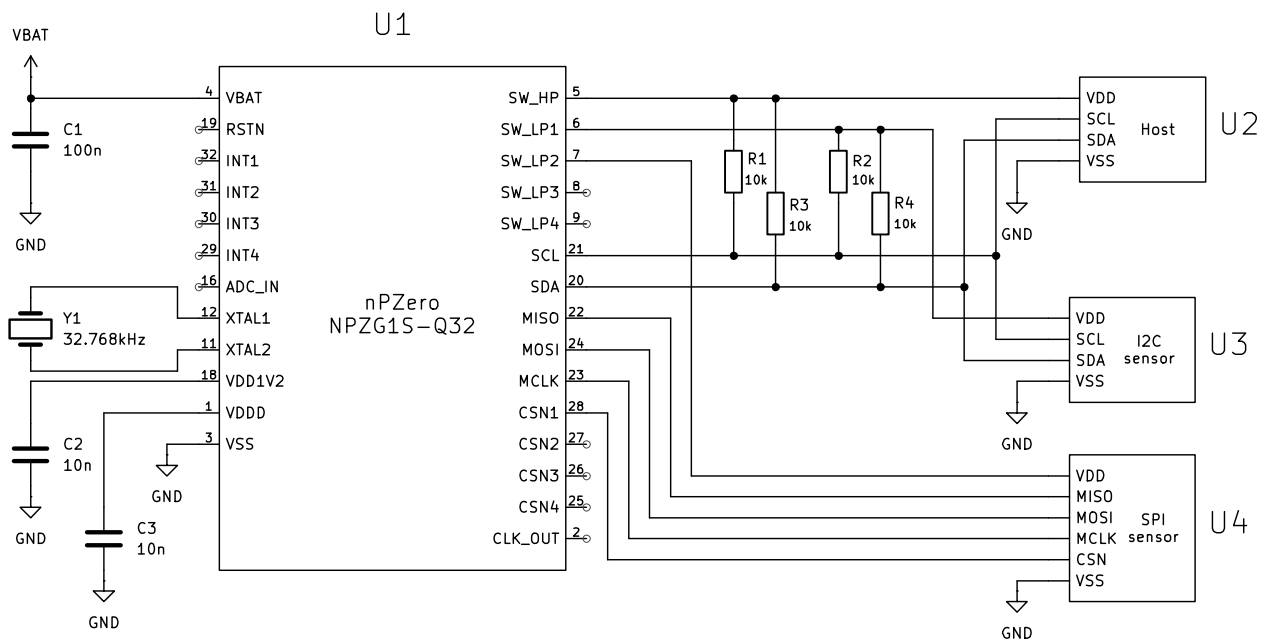


Figure 4: nPZero G1 typical application

Table 11: nPZero G1 external components

Symbol	Parameter	Required	Min	Typ	Unit
C <sub>1</sub>	VBAT capacitor	✓	10	100	nF
C <sub>2</sub>	VDD1V2 bypass capacitor	✓	2.0	10	nF
C <sub>3</sub>	VDDD bypass capacitor	✓	7.5	10	nF
R <sub>1</sub> -R <sub>4</sub>	Pull-up resistor		4.7k	10k	Ω
Y <sub>1</sub>	Crystal		-	32.768	kHz

## 2 Operation

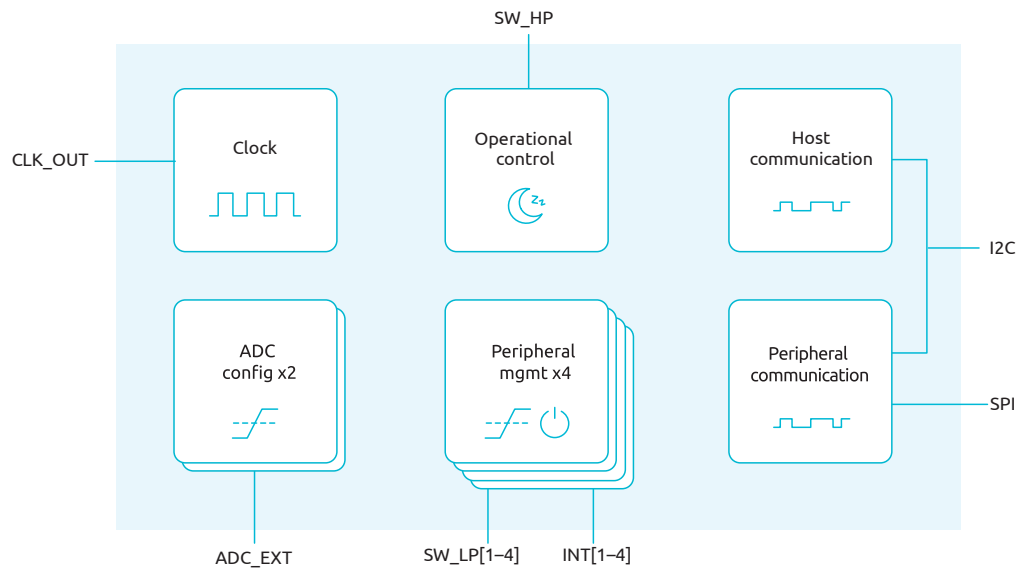


Figure 5: nPZero G1 logical block diagram.

The nPZero G1 can be divided into several logical blocks, as shown in Figure 5:

- **Host communications** – When operating as an I<sup>2</sup>C slave device, this block is used for receiving configuration parameters from the host and sending the current status to the host.
- **Operation control** – nPZero power state control, wake-up conditions, and reset, as well as the host power switch.
- **Peripheral management** – External peripheral configuration, power management, output value comparison and trigger conditions, and interrupt pin setup.
- **Peripheral communications** – External peripheral communication via SPI or I<sup>2</sup>C, peripheral initialization, and data retrieval.
- **ADC configuration** – Trigger conditions and value comparison for ADC channels.
- **Clock configuration** – Clock source selection and division.

## 2.1 Host Communication

After a reset, the device enters Standby state, during which it operates as an I<sup>2</sup>C slave device, with a 7-bit I<sup>2</sup>C address of 0x3D, and supporting communication speeds of up to 100 kbit/s.

In this state the host can read and write to the available nPZero registers, and the SRAM memory space, as described in *subsection 3.1 Register Map*.

A write or read operation is always preceded by a write operation with the data byte set to the target register to be written or read. For a register write, the next data byte will set the data to be written to the register. For a register read, a repeated start sequence is sent before a read operation, thereafter the device will output the register data on the SDA line.

The device also supports multi-byte reads and writes, as shown in Figure 6 and Figure 7.

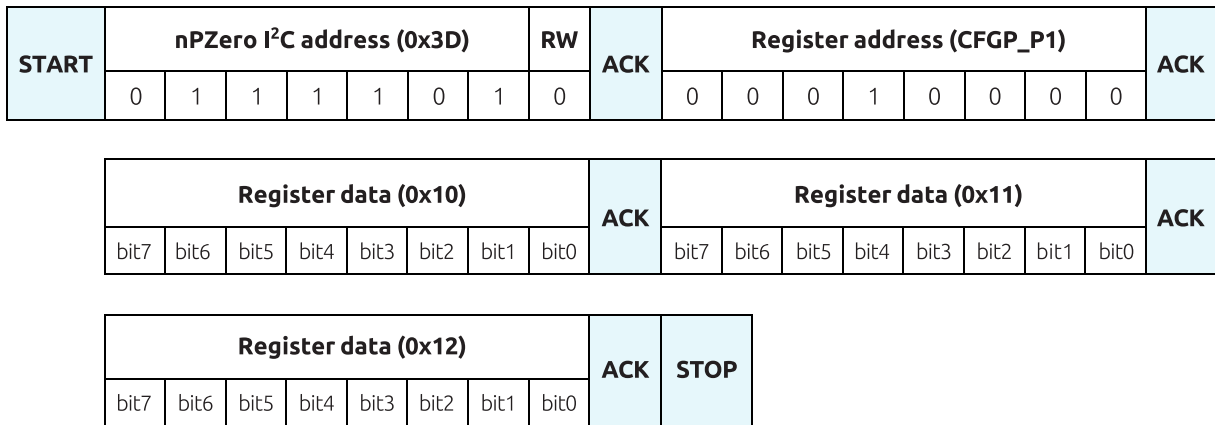


Figure 6: Example I<sup>2</sup>C multi-byte write operation on the nPZero G1

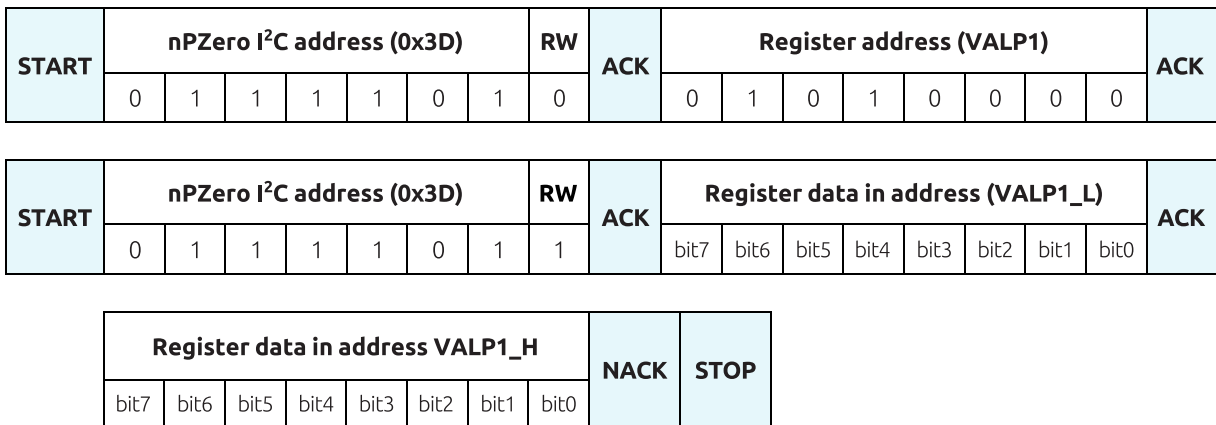


Figure 7: Example I<sup>2</sup>C multi-byte read operation on the nPZero G1

## 2.2 Operation Control

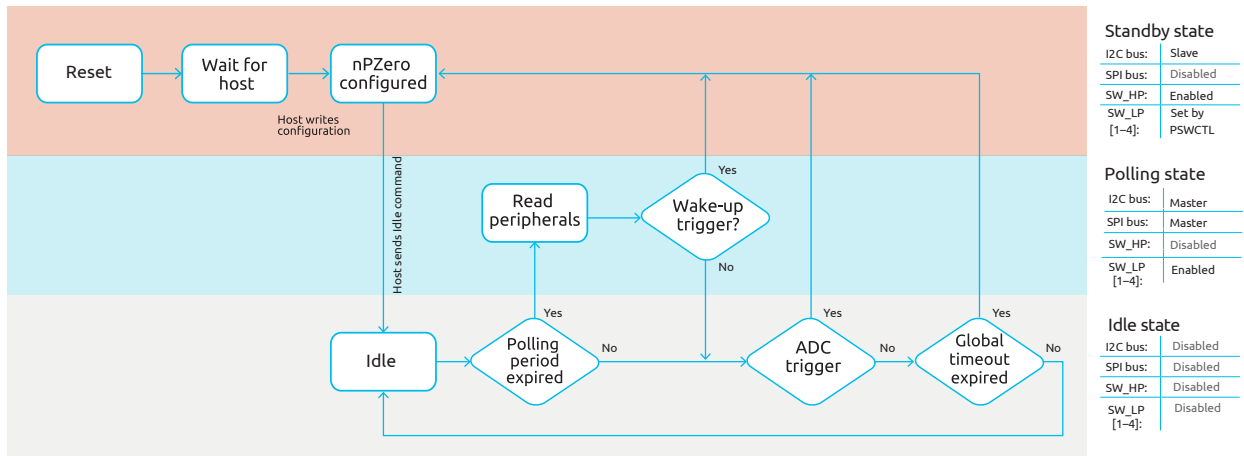


Figure 8: nPZero G1 decision flow chart and operation states

During normal operation, the nPZero G1 will alternate through different operations states, which in turn control the state of the host and peripheral switches, as well as the communication buses.

The nPZero G1 has the following operation states, as detailed in Figure 8:

- Standby state** – This is the default state after a reset. In this state the host switch control is enabled, and the device operates as an I<sup>2</sup>C slave. This allows the host to read/write to the configuration registers and SRAM, as well as switch to Idle state. The MCU needs to configure the nPZero only once in the very beginning in Standby state without repeatedly reconfiguring the nPZero every loop. If it is necessary, the MCU is able to reconfigure/change configurations in Standby state.
  - Idle state** – In this state the host switch is disabled, as well as the peripheral switches (unless configured as always-on), ADC sampling remains enabled, while bus communication is disabled on both I<sup>2</sup>C and SPI buses. The device will use its internal system clock for timekeeping and wait until the configured polling period expires to communicate with peripherals.
- The device may also switch to Standby state (i.e. wake-up) after a pre-defined amount of time (global timeout), ADC trigger event, or asynchronous interrupt event if so configured.
- Polling state** – At the specified polling periods, the nPZero will enable the corresponding peripheral power switch, initialize the peripheral via I<sup>2</sup>C or SPI depending on configuration, and either read back data through the same bus and compare against a threshold, or await an interrupt event to occur within a specified period of time. If a trigger event happens, the device may wake up and switch to Standby state or enter the Idle state again.

In Figure 9 a typical operation cycle is shown, annotating the different states at each point.

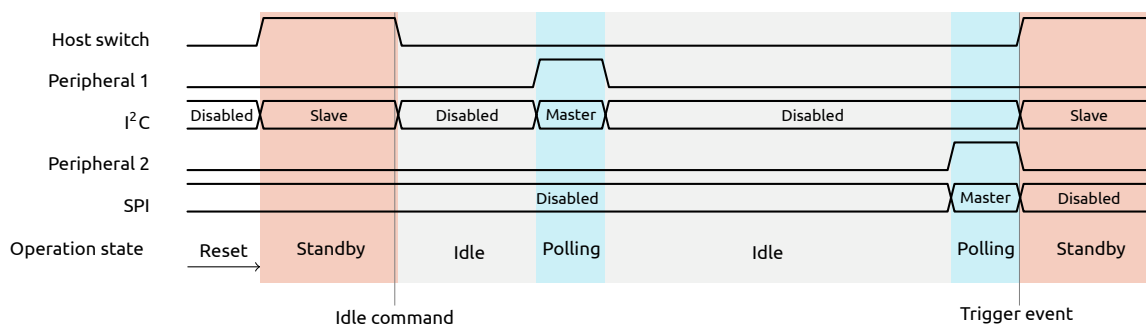


Figure 9: Example timing diagram highlighting different operation states

## 2.2.1 Wake-up Sources

Depending on the configuration, the following conditions can cause the device to wake-up from Idle state:

- **Peripheral or ADC trigger** – If the read value of a peripheral or ADC meets the trigger criteria (see 2.3.5 *Trigger Conditions and Wake-up*), or in the event of a peripheral interrupt (see 2.3.6 *Interrupt Pins*).  
To enable a peripheral or ADC input as a wake-up source, the corresponding bits must be set in WUP\_P[1-4] or WUP\_A[1-2] register fields.
- **Peripheral I<sup>2</sup>C NAK event** – In the event of a not acknowledge (NAK) during I<sup>2</sup>C communication with a peripheral.  
To enable wake-up on NAK, I<sup>2</sup>C communication must be enabled via the SPIEN\_P[1-4] register field, and the WUNAK\_P[1-4] register field must be set.
- **Global timeout** – In the absence of other events, the device will wake-up from Idle state after the time period defined in the TOUT register.

If multiple wake-up sources are set in WUP\_P[1-4] or WUP\_A[1-2], then the WUPMOD field in the SYSCFG1 register will determine if a trigger event in any of the wake-up sources is sufficient to wake-up the device, or if all of the wake-up sources must trigger for a wake-up.

The STA1 and STA2 registers can be read to determine the cause of the wake-up event.

## 2.2.2 Reset

The device will go through a power-on reset cycle when the supply voltage on the VBAT pin rises above a threshold of approximately 1.2 V. During a power-on-reset cycle, the internal references and oscillators will start up, and when the internal supplies have stabilized, the internal digital core will be reset, the default register configuration will be loaded, and the host power switch output enabled, at which point the nPZero is ready to accept communication from the host.

In addition, there are two other reset types:

- **External reset** – By pulling the RSTN pin low, an external reset is asserted, triggering a full restart of the device which should be equivalent to a power-down/power-up or brown-out reset. During reset, the nPZero will load the default register configuration. When the RSTN pin is low the internal oscillators, references and digital blocks will be disabled.
- **Software reset** – By sending 0xA5 to the SLEEP\_RST register, a software reset is started. This will load the default digital core configuration only. This operation will disable the CLK\_OUT pin to its default value.

**NOTE:** During an external or software reset, the host power switch output, i.e. SW\_HP pin, will be disabled, becoming high impedance.

The RST\_SRC register field can be read to determine the reset source of the nPZero.

## 2.3 Peripheral Management

Control of whether a peripheral is enabled or not is done by changing the power mode through the PWMOD\_P[1-4] field in the CFGP\_P[1-4] register (see Table 28 'Peripheral power modes'). There are three different power modes available:

- **Disabled** – Peripheral is not powered on.
- **Periodic power-on** – Peripheral is enabled periodically as set by the PERP[1-4] register.
- **Always-on** – Peripheral is always powered-on.

### 2.3.1 Power Switch

The behavior of the power switch peripheral outputs, i.e. the SW\_LP[1-4] pins, can be set to either a power output that can supply the peripheral directly, or a logic output with configurable polarity to control an external power switch.

Power switch configuration is defined in the PSWMOD\_P[1-4] field in the CFGP[1-4] register, see also Table 30 'Peripheral power switch mode'.

When the device is in Standby state, the state of the power switch output is directly controlled by the PSWINT\_P[1-4] fields in the PSWCTL register. By default, all peripheral power switches are disabled after a reset.

### 2.3.2 Polling Modes

To accommodate a wide range of peripherals, the nPZero supports several different modes that can make use of I<sup>2</sup>C or SPI to initialize the peripherals, read data values to compare against thresholds, see 2.3.5 'Trigger Conditions and Wake-up', and respond to peripheral interrupts.

For peripherals that do not require initialization, it is also possible to trigger solely on peripheral interrupts or read data directly.

The SW\_LP[1-4] pins can either be always-on or periodically powered on via the PWMOD\_P[1-4] field in CFGP[1-4] register. For simplicity, the following polling mode examples have the periodic power-on option selected.

- **Polling Mode 0** – Periodically initialize via I<sup>2</sup>C or SPI, read data value, and compare against threshold
- **Polling Mode 1** – Periodically initialize via I<sup>2</sup>C or SPI, wait on sensor interrupt until timeout, read data value, and compare against thresholds
- **Polling Mode 2** – Periodically initialize via I<sup>2</sup>C or SPI, trigger on sensor interrupt until timeout
- **Polling Mode 3** – Trigger on sensor interrupt

**Polling Mode 0** – When a peripheral is set to Mode 0, the device will periodically power up the peripheral, wait for some time (defined by *t<sub>init</sub>*), and send initialization commands via I<sup>2</sup>C or SPI. The device then reads the sensor values after some time (defined by *t<sub>wait</sub>*), to accommodate for peripherals with low sampling rates. After the values are read, they are compared against the set threshold, and if exceeded, the device is triggered and the host is powered up.

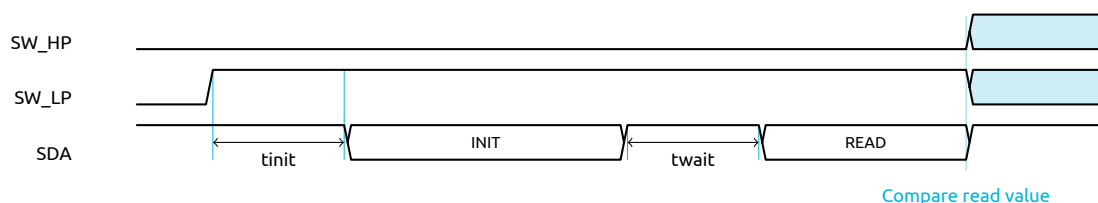


Figure 10: Timing diagram for Polling Mode 0

**Polling Mode 1** – When a peripheral is set to Mode 1, the device will periodically power up the peripheral, wait for some time (defined by *tinit*), and send initialization commands via I<sup>2</sup>C or SPI. The device then waits for a peripheral interrupt to be asserted, before reading the sensor values to accommodate for peripherals which support *data ready* type interrupts. After the values are read, they are compared against the set thresholds, and if exceeded, the device is triggered and the host is powered up. If the peripheral does not assert an interrupt within a certain amount of time (defined by *twait*), the peripheral is powered off.

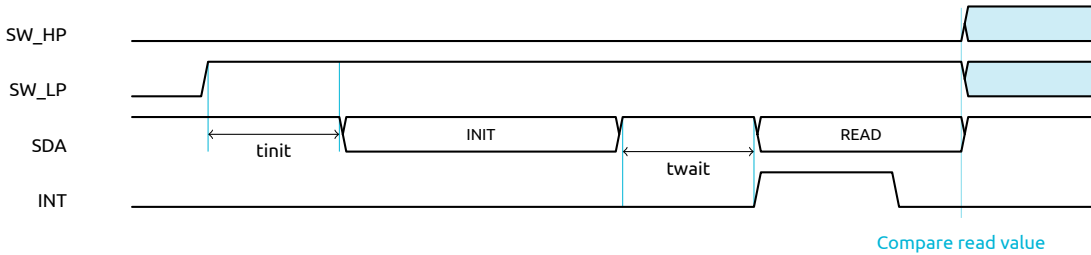


Figure 11: Timing diagram for Polling Mode 1

**Polling Mode 2** – When a peripheral is set to Mode 2, the device will periodically power-up the peripheral, wait for some time (defined by *tinit*), and send initialization commands via I<sup>2</sup>C or SPI. The device then waits for a peripheral interrupt to be asserted at which point the device is triggered and the host is powered up. This mode can be used with peripherals that support internal comparison against set thresholds, and in this case the initialization commands are expected to set these parameters. If the peripheral does not assert an interrupt within a certain amount of time (defined by *twait*), then the peripheral is powered off.

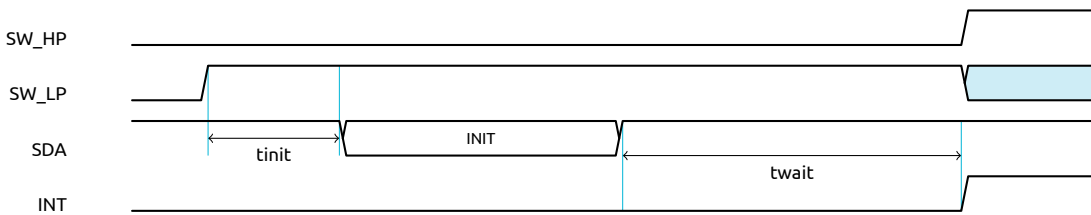


Figure 12: Timing diagram for Polling Mode 2

**Peripheral Mode 3** When a peripheral is set to Mode 3, if SW\_LP is always on, the device will wake asynchronously when a peripheral interrupt is asserted. If SW\_LP in periodic power-on then the device will periodically power up the peripheral and wait for a peripheral interrupt to be asserted, at which point the device is triggered and the host is powered up. If the peripheral does not assert an interrupt within a certain amount of time (defined by *twait*), then the peripheral is powered off. This mode can be used with simple peripherals which do not need any setup.

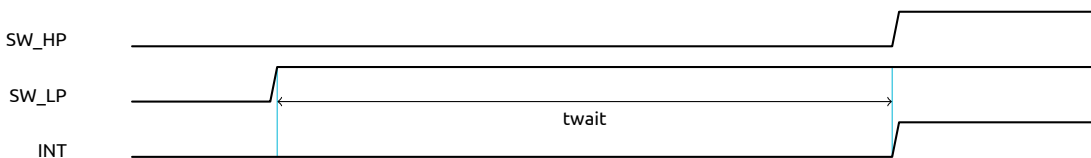


Figure 13: Timing diagram for Polling Mode 3

### 2.3.3 Wait Times

As described above, there are two configurable wait times that will impact the peripheral polling behavior: *tinit* and *twait*. These wait times can be enabled or disabled using the TINIT\_EN\_P[1-4] and TWT\_EN\_P[1-4] fields in the TCFGP1-4] register.

The actual amount of time to wait during *tinit* and *twait* depends on the value of the TWTP[1-4] register which by default is defined in units of 256 periods of the internal 400kHz oscillator.

By setting the TINIT\_EXT\_P[1-4] and/or TWT\_EXT\_P[1-4] fields of the TCFGP[1-4] register, the value of TWTP[1-4] can be interpreted as 4096 periods of the internal 400kHz oscillator, thereby extending *tinit* or *twait*, respectively.

### 2.3.4 Data Values

If the device is configured to read data from the peripheral, the expected data type can be set in the DTYPE\_P[1-4] register field in the MODP[1-4] register. This can be 16-bit signed, 16-bit unsigned, or 8-bit unsigned integers.

After a wake-up event, the last value read from the peripheral can be read from the VALP[1-4] registers.

### 2.3.5 Trigger Conditions and Wake-up

The trigger conditions for each peripheral can be either an external interrupt signal or a comparison between the read data from the peripheral and set thresholds.

The thresholds are defined using over- and under-values, defined in the THROVP[1-4] and THRUNP[1-4] registers respectively. These registers are 16-bits wide, however their values should match the data type set in DTYPE\_P[1-4].

There are two threshold-compare-modes where a wake-up trigger event happens when either the value is above or equal to the over-threshold, or below or equal to the under-threshold (default trigger area), or when the value goes below the over-threshold and above the under-threshold (inverted trigger area), see Figure 14 for an illustration of the trigger conditions. The trigger conditions are selected by the CMOD\_P[1-4] field in the MODP[1-4] register.

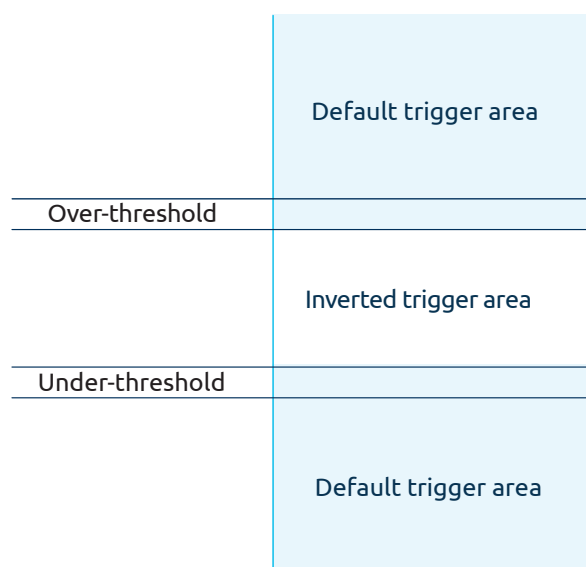


Figure 14: Trigger area of threshold-compare-modes

### 2.3.6 Interrupt Pins

An interrupt pin is associated with each peripheral, for a total of four pins (INT[1-4]). Each interrupt pin can be configured through the INTMOD\_P[1-4] field in the CFGP[1-4] register, to act as either:

- **Interrupt input** – Can be connected to a peripheral logical output to signal a data-ready condition or a trigger event;
- **Trigger output** – Will be asserted when a trigger condition happens on the configured peripheral.

Each interrupt pin has internal pull-up resistors with configurable strength that can be enabled through the INTCFG register fields. The pull-up is enabled by default.

## 2.4 Peripheral Communication

The nPZero supports I<sup>2</sup>C and SPI serial protocols to communicate with external peripherals. Two distinct communication steps are supported:

- **Initialization** – Data is sent to the peripheral in order to configure or initialize it. No data is read.
- **Read values** – Data is requested from the peripheral either by reading certain registers via I<sup>2</sup>C or by shifting data out via SPI. The received data is then stored in the VALP[1-4] registers.

The communication protocol choice for each peripheral can be defined through the SPIEN\_P[1-4] field in the ADDR\_P[1-4] register.

### 2.4.1 SRAM Structure

The internal 128-byte SRAM is used to store peripheral initialization commands and data to be shifted out in SPI mode when reading data values from the peripheral. The SRAM data structure will change depending on the selected communication protocol. Figure 15 provides an example of how the data should be structured in the SRAM, depending on the chosen communication protocol.

The SRAM data boundaries for each peripheral are calculated based on the registers that define the number of commands for each peripheral. This means that when configuring multiple peripherals, the data must be written to the SRAM sequentially without gaps.

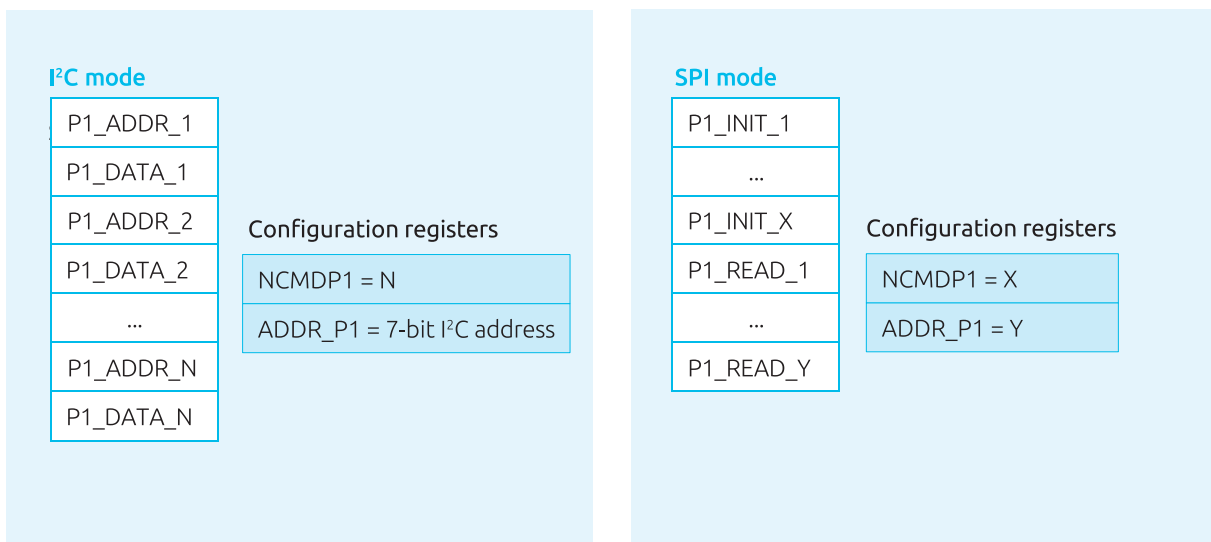


Figure 15: nPZero G1 SRAM data structure for I<sup>2</sup>C and SPI modes

## 2.4.2 I<sup>2</sup>C

**Peripheral initialization** For I<sup>2</sup>C peripherals, the initialization commands are stored in the SRAM as address and data byte pairs. The device will send an I<sup>2</sup>C write command followed by the peripheral register address to be written, and then the data to be written to that address. The number of address/data byte pairs (number of commands) must be defined in the NCM DP[1-4] register. Supported I<sup>2</sup>C frequency is 100 kHz.

**Reading data** To read data from the peripheral, the RREGP[1-4] register defines the peripheral register address to be read. If the data type is set to 16-bit signed or 16-bit unsigned, then this address is assumed to be the lower byte, and for the higher byte the address is incremented by one.

**Multi-byte transfers** Multi-byte transfers are supported when the addresses to be written are sequential, and this mode can be enabled through the SEQRW\_P[1-4] field in the MODP[1-4] register. In this mode, when the device sees the next address to send as sequential, it only sends the next data byte. When a non-sequential address is encountered, an I<sup>2</sup>C restart command is sent, and thereafter the next address byte. This applies during both initialization and data-read steps.

**NAK and retries** In the case of a peripheral NAK, the polling operation can continue in one of the following ways:

- **Ignore and continue** – The peripheral polling will be skipped for this period and the nPZero will enter Idle state again until the next polling period. This is the default behavior.
- **Wake-up** – If the WUNAK\_P[1-4] field in the MODP[1-4] register is set, the device will wake-up if a NAK condition is encountered during communication.
- **Retry** – If the I2CRET\_P[1-4] field in the TCFGP[1-4] register is set to a value other than 0, the device will retry communication for the number of times specified. If the peripheral acknowledges eventually, the polling will continue as normal. Otherwise, it will either wake-up, or ignore and continue depending on the value of the WUNAK\_P[1-4] register field.

## 2.4.3 SPI

**SPI modes** Standard SPI modes are supported (CPOL/CPHA) as shown in Figure 16. The SPI mode can be configured in the SPIMOD\_P[1-4] field in the MODP[1-4] register, see *Table 34 'SPI mode configuration'*. Supported SPI frequency is 100 kHz.

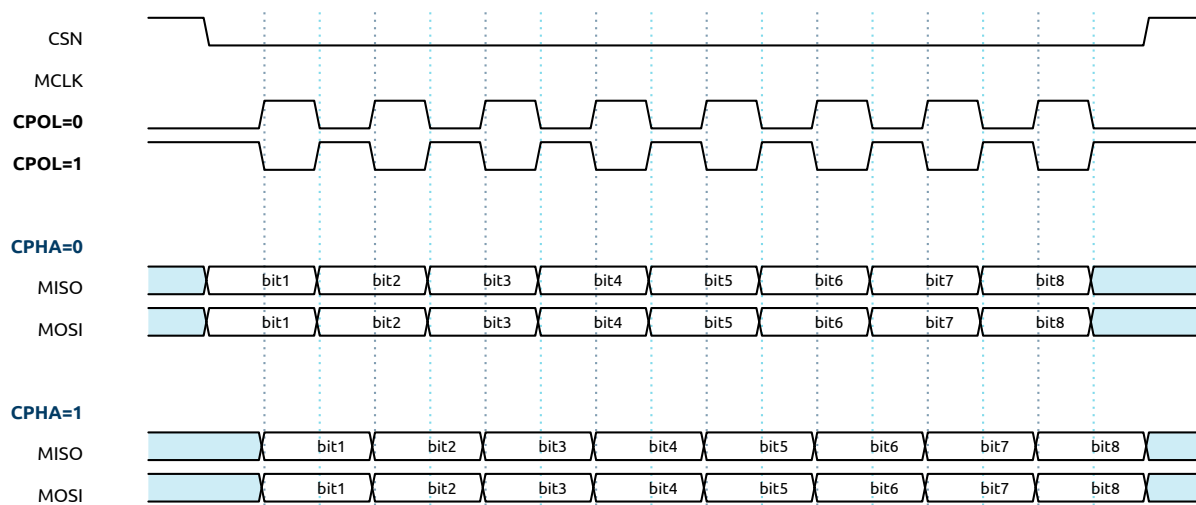


Figure 16: Standard SPI modes diagram. The dashed lines represent where data is sampled. If CPHA=0 the first data bit is sampled on the next MCLK transition; if CPHA=1 the first data bit is sampled on the second MCLK transition.

**Peripheral initialization** For SPI peripherals, the SRAM data is the data to be shifted out to the peripheral. The number of bytes to be shifted during the initialization phase is defined in the NCMDP\_P[1-4] field in the NCMDP[1-4] register. Typical SPI initialization is demonstrated in Figure 17.

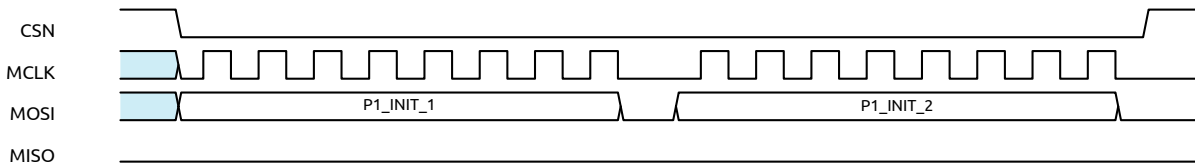


Figure 17: Typical SPI initialization of a peripheral using SPI mode 0

**Reading data** Similar to the initialization sequence, the data to be shifted out to the peripheral during read mode, such that the peripheral shifts out the values to be read. This data should be written to SRAM directly after the initialization data. The number of bytes to be shifted during the read phase is defined in ADDR\_P[1-4] field in the ADDR\_P[1-4] register. The last byte (or two bytes in case of 16-bit data) shifted into the nPZero is stored in the VALP[1-4] registers. Typical reading data using SPI mode 0 is shown in Figure 18.

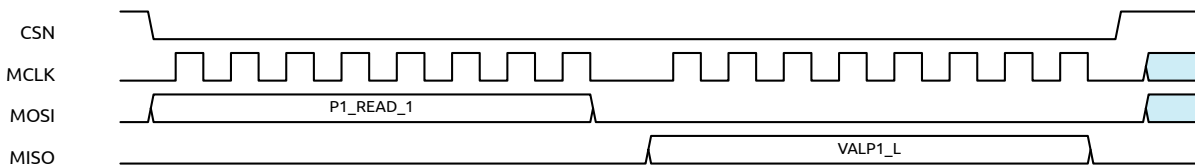


Figure 18: Typical SPI read of a peripheral using SPI mode 0. The illustration shows an example with one read command and 8-bit peripheral data.

### 2.4.4 Data Register Swapping

For specific scenarios such as peripherals with 16-bit registers, the device can swap the high and low bytes of the 16-bit value read from the peripheral for the data to be correctly compared against the thresholds. This can be enabled through the SWPRREG\_P[1-4] field in the MODP[1-4] register.

### 2.4.5 I/O Pin Control

The behavior of both SPI and I<sup>2</sup>C pins when inactive can be controlled to avoid possible leakage currents through the pins of the peripherals when power is disabled.

The I<sup>2</sup>C pins SDA and SCL pins can use internal pull-ups by setting the I2C\_PUP\_EN field, and these pull-ups can be automatically disabled when the I<sup>2</sup>C bus is not in use by additionally setting I2C\_PUP\_AUTO.

For SPI, the CSN[1-4], MOSI, and MCLK output pins can be set to high impedance when not in use, by setting the SPI\_AUTO field.

## 2.5 ADC Configuration

The nPZero contains an ADC with two channels, one internally connected to VBAT, and one externally connected to the ADC\_IN pin. The internal ADC channel is always enabled while the external ADC input can be enabled through the ADC\_EXT\_ON register field.

The ADC sampling rate is determined by the system clock or the crystal oscillator with a division factor applied, see *2.6 ADC Sampling Rate* for more details.

### 2.5.1 Trigger Conditions and Wake-up

The trigger condition for wake-up from the ADC channels is a data comparison to a set threshold. The thresholds are set using over- and under-values independently for each channel, defined in the THROVA[1-2] and THRUNA[1-2] registers respectively.

A trigger condition happens when the ADC value goes above or equal the over-threshold, or below or equal the under-threshold.

A trigger event happens when a trigger condition is met and the corresponding ADC channel is set as a wake-up source in the WUP\_A[1-2] field in the SYSCFG1 register.

### 2.5.2 Data Values

After a wake-up event, i.e. device in Standby state, the last value read from the ADC channels can be read from the ADC\_CORE and ADC\_EXT registers, respectively for internal and external channels.

To correlate the ADC values with its input voltage, see *Table 50 'ADC codes'*.

## 2.6 Clock Configuration

The nPZero G1 includes an internal low-power oscillator, which is the default clock source. The device also includes a crystal oscillator (XO) that can be optionally enabled if higher precision is required or to output a clock via the CLK\_OUT pin.

### 2.6.1 System Clock

The system clock can be derived from two internal clock sources: a 10 Hz low-power oscillator, or a 32.768 kHz XO divided by 2048 resulting in 16Hz, see Figure 19.

The system clock source is controlled by the SCLK\_SEL field in the SYSCFG2 register. It is also possible to further divide this clock through the SCLK\_DIV\_EN and SCLK\_DIV fields in the SYSCFG2 register. Depending on the clock source selected, either the low-power oscillator or the crystal oscillator, the system clock frequencies can go from 0.625 to 10 Hz or 1 to 16 Hz respectively.

Due to the low frequencies of either clock source, changing SCLK\_SEL register field will not have an immediate effect as edge synchronization needs to occur. The clock source in use by the device can be read from the SCLK\_SEL\_STATUS field in the SYSCFG3 register. When SCLK\_SEL\_STATUS matches SCLK\_SEL, the clock source change is complete.

### 2.6.2 ADC Sampling Rate

The ADC sampling rate is by default derived from the system clock, or alternatively from the XO divided by a programmable factor as illustrated in Figure 20. Depending on the clock source selected, the system clock or the crystal oscillator, the ADC sampling clock frequencies can go from 0.625 to 16 Hz or 64 Hz to 1024 Hz respectively.

The ADC sampling clock source can be selected through the ADC\_CLK\_SEL field in the SYSCFG2 register. Please note that to use the ADC sampling rate derived from the XO, the SCLK\_SEL field needs to be set to 1 to enable the XO.

When the external ADC channel is enabled, the sampling of each channel becomes interleaved, effectively halving the sample rate of each channel.

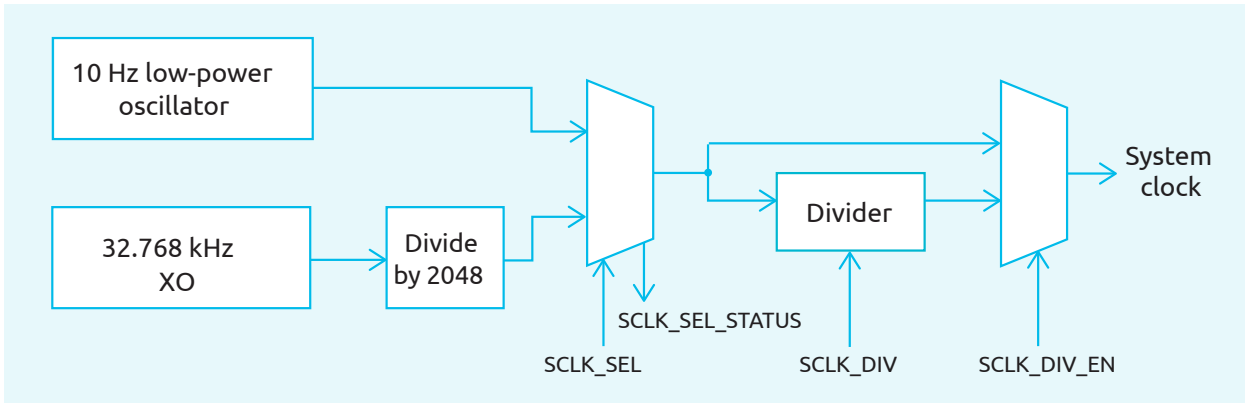


Figure 19: nPZero G1 system clock routing diagram

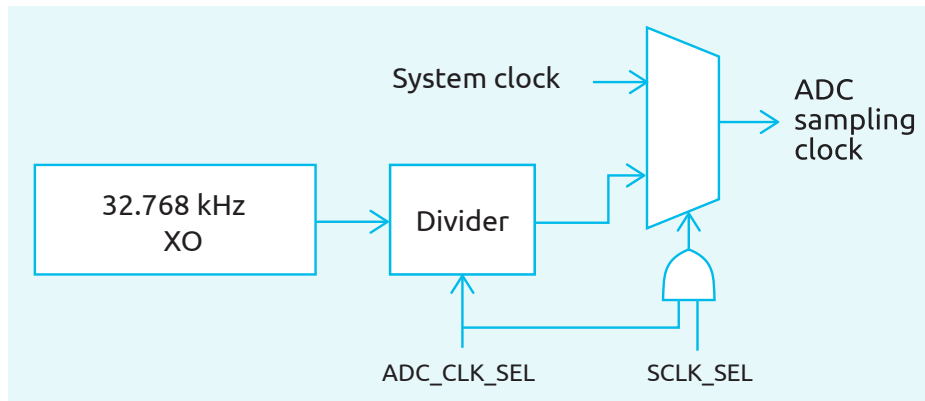


Figure 20: nPZero G1 ADC sampling clock routing diagram

### 2.6.3 Crystal Oscillator Clock Output

To enable the internal crystal oscillator, an external crystal needs to be connected to the XTAL1 and XTAL2 pins. The crystal oscillator clock output can be routed through a divider to the CLK\_OUT pin which will output a nominal 32.768 kHz clock signal. The CLK\_OUT output can be controlled through the XO\_CLKOUT\_DIV field in the SYSCFG3 register.

The crystal oscillator will be enabled whenever SCLK\_SEL or XO\_CLKOUT\_DIV are set, will remain enabled regardless of the nPZero operational state, and when enabled can result in increased power consumption.

See *Table 24 'CLK\_OUT clock selection'* for setting different clock frequencies. The CLK\_OUT pin is disabled by default.

## 3 Registers

### 3.1 Register Map

Addr	Register	Type	Register Field							
			7	6	5	4	3	2	1	0
0x00	IDLE_RST	R/W	IDLE_RST							
0x01	ID	R	ID							
0x02	STA1	R	FTOUT	FA1	FA2	–	RST_SRC			
0x03	STA2	R	FNAK_P4	FP4	FNAK_P3	FP3	FNAK_P2	FP2	FNAK_P1	FP1
0x04	PSWCTL	R/W	PSW_VN_ON	PSW_EN_VN	PSWH_MODE		PSWINT_P4	PSWINT_P3	PSWINT_P2	PSWINT_P1
0x05	SYSCFG1	R/W	–	WUPMOD	WUP_A2	WUP_A1	WUP_P4	WUP_P3	WUP_P2	WUP_P1
0x06	SYSCFG2	R/W	–	ADC_CLK_SEL		ADC_EXT_ON	SCLK_SEL	SCLK_DIV		SCLK_DIV_EN
0x07	SYSCFG3	R/W	SCLK_SEL_STA-TUS	XO_CLKOUT_DIV			SPI_AUTO	I2C_PUP_AUTO	I2C_PUP_EN	IO_STR
0x08	TOUT	R/W	TOUT_L							
0x09			TOUT_H							
0x0A	INTCFG	R/W	PU_S_INT4	PU_INT4	PU_S_INT3	PU_INT3	PU_S_INT2	PU_INT2	PU_S_INT1	PU_INT1
0x10	CFGP1	R/W	INTMOD_P1		PSWMOD_P1		TMOD_P1		PWMOD_P1	
0x11	MODP1	R/W	SPIMOD_P1		SWPRREG_P1	WUNAK_P1	SEQRW_P1	DTYPE_P1		CMOD_P1
0x12	PERP1	R/W	PERP1_L							
0x13			PERP1_H							
0x14	NCMDP1	R/W	–	NCMD_P1						
0x15	ADDRP1	R/W	SPIEN_P1	ADDR_P1						
0x16	RREGP1	R/W	RREGP1							
0x17	THROVP1	R/W	THROVP1_L							
0x18			THROVP1_H							
0x19	THRUNP1	R/W	THRUNP1_L							
0x1A			THRUNP1_H							
0x1B	TWTP1	R/W	TWTP1							
0x1C	TCFGP1	R/W	–	I2CRET_P1		TINIT_EXT_P1	TINIT_EN_P1	TWT_EXT_P1	TWT_EN_P1	
0x1D	CFGP2	R/W	INTMOD_P2		PSWMOD_P2		TMOD_P2		PWMOD_P2	
0x1E	MODP2	R/W	SPIMOD_P2		SWPRREG_P2	WUNAK_P2	SEQRW_P2	DTYPE_P2		CMOD_P2

Addr	Register	Type	Register Field							
			7	6	5	4	3	2	1	0
0x1F	PERP2	R/W	PERP2_L							
0x20			PERP2_H							
0x21	NCMDP2	R/W	-	NCMD_P2						
0x22	ADDRP2	R/W	SPIEN_P2	ADDR_P2						
0x23	RREGP2	R/W	RREGP2							
0x24	THROVP2	R/W	THROVP2_L							
0x25			THROVP2_H							
0x26	THRUNP2	R/W	THRUNP2_L							
0x27			THRUNP2_H							
0x28	TWTP2	R/W	TWTP2							
0x29	TCFGP2	R/W	-	I2CRET_P2	TINIT_EXT_P2	TINIT_EN_P2	TWT_EXT_P2	TWT_EN_P2		
0x2A	CFGP3	R/W	INTMOD_P3	PSWMOD_P3	TMOD_P3		PWMOD_P3			
0x2B	MODP3	R/W	SPIMOD_P3	SWPRREG_P3	WUNAK_P3	SEQRW_P3	DTYPE_P3		CMOD_P3	
0x2C	PERP3	R/W	PERP3_L							
0x2D			PERP3_H							
0x2E	NCMDP3	R/W	-	NCMD_P3						
0x2F	ADDRP3	R/W	SPIEN_P3	ADDR_P3						
0x30	RREGP3	R/W	RREGP3							
0x31	THROVP3	R/W	THROVP3_L							
0x32			THROVP3_H							
0x33	THRUNP3	R/W	THRUNP3_L							
0x34			THRUNP3_H							
0x35	TWTP3	R/W	TWTP3							
0x36	TCFGP3	R/W	-	I2CRET_P3	TINIT_EXT_P3	TINIT_EN_P3	TWT_EXT_P3	TWT_EN_P3		
0x37	CFGP4	R/W	INTMOD_P4	PSWMOD_P4	TMOD_P4		PWMOD_P4			
0x38	MODP4	R/W	SPIMOD_P4	SWPRREG_P4	WUNAK_P4	SEQRW_P4	DTYPE_P4		CMOD_P4	

Addr	Register	Type	Register Field							
			7	6	5	4	3	2	1	0
0x39	PERP4	R/W	PERP4_L							
0x3A			PERP4_H							
0x3B	NCMDP4	R/W	–	NCMD_P4						
0x3C	ADDRP4	R/W	SPIEN_P4	ADDR_P4						
0x3D	RREGP4	R/W	RREGP4							
0x3E	THROVP4	R/W	THROVP4_L							
0x3F			THROVP4_H							
0x40	THRUNP4	R/W	THRUNP4_L							
0x41			THRUNP4_H							
0x42	TWTP4	R/W	TWTP4							
0x43	TCFGP4	R/W	–	I2CRET_P4		TINIT_EXT_P4	TINIT_EN_P4	TWT_EXT_P4	TWT_EN_P4	
0x44	THROVA1	R/W	–			THROVA1				
0x45	THRUNA1	R/W	–			THRUNA1				
0x46	THROVA2	R/W	–			THROVA2				
0x47	THRUNA2	R/W	–			THRUNA2				
0x50	VALP1	R	VALP1_L							
0x51			VALP1_H							
0x52	VALP2	R	VALP2_L							
0x53			VALP2_H							
0x54	VALP3	R	VALP3_L							
0x55			VALP3_H							
0x56	VALP4	R	VALP4_L							
0x57			VALP4_H							
0x58	ADC_CORE	R	–			ADC_CORE				
0x59	ADC_EXT	R	–		ADC_EXT					
0x80	SRAM	R/W	–							
0xFF										

### 3.2 Register Description

#### 3.2.1 IDLE\_RST

Bit	7	6	5	4	3	2	1	0
<b>0x00</b>	<b>IDLE_RST</b>							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 12: IDLE\_RST register description

<b>IDLE_RST</b>	When set to 0xFF, the nPZero will enter Idle mode, shutting down the host power and assuming control of the I <sup>2</sup> C bus. When set to 0xA5, the nPZero will perform a soft reset.
-----------------	--

#### 3.2.2 ID

Bit	7	6	5	4	3	2	1	0
<b>0x01</b>	<b>ID</b>							
Type	R	R	R	R	R	R	R	R
Reset	0	1	1	0	0	0	0	0

Table 13: ID register description

<b>ID</b>	The device identification field for the nPZero G1 is <b>0x60</b> .
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#### 3.2.3 STA1

Bit	7	6	5	4	3	2	1	0
<b>0x02</b>	<b>FTOUT</b>	<b>FA1</b>	<b>FA2</b>	<b>-</b>	<b>RST_SRC</b>			
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	1

Table 14: STA1 register description

<b>RST_SRC</b>	Indicates the reason for the reset, see <i>Table 15 'Reset source'</i> .
<b>FA2</b>	When flag is set to 1, it indicates the external ADC channel (connected to ADC_IN) was triggered.
<b>FA1</b>	When flag is set to 1, it indicates the internal ADC channel (connected to VBAT) was triggered.
<b>FTOUT</b>	When flag is set to 1, it indicates the wake-up reason was a global time-out before any other wake-up source was triggered.

Table 15: Reset source

<b>RST_SRC</b>	<b>Reset source</b>
X001	Power-on reset occurred.
X010	External reset occurred (via RSTN pin).
X100	Brown-out reset occurred.
1XXX	Soft reset occurred (via an I <sup>2</sup> C command).

### 3.2.4 STA2

Bit	7	6	5	4	3	2	1	0
0x03	<b>FNAKP4</b>	<b>FP4</b>	<b>FNAKP3</b>	<b>FP3</b>	<b>FNAKP2</b>	<b>FP2</b>	<b>FNAKP1</b>	<b>FP1</b>
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Table 16: STA2 register description

<b>FP1</b> <b>FP2</b> <b>FP3</b> <b>FP4</b>	When the flag is set to 1, it indicates the corresponding peripheral was triggered.
<b>FNAKP1</b> <b>FNAKP2</b> <b>FNAKP3</b> <b>FNAKP4</b>	When the flag is set to 1, it indicates the corresponding peripheral did not acknowledge. If WUNAK_P[1-4] is active then FNAKP[1-4] will trigger a wake-up.

### 3.2.5 PSWCTL

Bit	7	6	5	4	3	2	1	0
0x04	<b>PSW_VN_ON</b>	<b>PSW_EN_VN</b>	<b>PSWH_MODE</b>	<b>PSWINT_P4</b>	<b>PSWINT_P3</b>	<b>PSWINT_P2</b>	<b>PSWINT_P1</b>	
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 17: PSWCTL register description

<b>PSWINT_P1</b> <b>PSWINT_P2</b> <b>PSWINT_P3</b> <b>PSWINT_P4</b>	Controls the peripheral power switch output state when the device is in Standby state.
<b>PSWH_MODE</b>	Sets the host power switch mode (SW_HP pin), see <i>Table 18 'Host power switch mode'</i> .
<b>PSW_EN_VN</b>	Feature not available in NPZG1S, do not set this field register. Enables power switches automatic gate boost for reduced $R_{ds(on)}$ .
<b>PSW_VN_ON</b>	When the flag is set to 1, indicates the gate boost is active.

Table 18: Host power switch mode

<b>PSWH_MODE</b>	<b>Pin mode</b>
00	Power switch mode (outputs VBAT or open)
01	Invalid
10	Logic output (High when host enabled)
11	Logic output inverted (Low when host enabled)

### 3.2.6 SYSCFG1

Bit	7	6	5	4	3	2	1	0
0x05	–	WUPMOD	WUP_A2	WUP_A1	WUP_P4	WUP_P3	WUP_P2	WUP_P1
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 19: SYSCFG1 register description

<b>WUP_P1</b> <b>WUP_P2</b> <b>WUP_P3</b> <b>WUP_P4</b>	Enables this peripheral as a wake-up source when triggered. (0: Peripheral does not wake-up system; 1: Peripheral can wake-up system)
<b>WUP_A1</b>	Enables the internal ADC channel trigger (VBAT pin) as a wake-up source. (0: ADC wake-up disabled; 1: ADC wake-up enabled)
<b>WUP_A2</b>	Enables the external ADC channel (ADC_IN pin) as a wake-up source. (0: ADC wake-up disabled; 1: ADC wake-up enabled)
<b>WUPMOD</b>	Controls if any wake-up source trigger is sufficient to wake-up the system, or if all wake-up source triggers are necessary to wake-up. (0: Wake-up system on any trigger; 1: Wake-up system on all triggers)

### 3.2.7 SYSCFG2

Bit	7	6	5	4	3	2	1	0
0x06	–	ADC_CLK_SEL	ADC_EXT_ON	SCLK_SEL	SCLK_DIV		SCLK_DIV_EN	
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 20: SYSCFG2 register description

<b>SCLK_DIV_EN</b>	Enables division of system clock, controlled by SCLK_DIV. (0: Disable clock division; 1: Enable clock division)
<b>SCLK_DIV</b>	Controls system clock divider, see <i>Table 21 'System clock divider'</i> .
<b>SCLK_SEL</b>	Controls system clock source between internal low-power oscillator or crystal oscillator. (0: Low-power oscillator; 1: Crystal oscillator)
<b>ADC_EXT_ON</b>	Enables external ADC input sampling (ADC_IN pin). When enabled, the sampling rates for both ADC channels (VBAT and ADC_IN) is halved. (0: Disable ADC_IN; 1: Enable ADC_IN)
<b>ADC_CLK_SEL</b>	Selects ADC sampling frequency, see <i>Table 22 'ADC clock selection'</i> . <b>NOTE:</b> For XO derived clocks the SCLK_SEL field must be set to 1.

Table 21: System clock divider

SCLK_DIV	Division ratio
00	Divide by 2
01	Divide by 4
10	Divide by 8
11	Divide by 16

Table 22: ADC clock selection

ADC_CLK_SEL	Selection
00	System clock
01	XO clock divided by 512 (64 Hz)
10	XO clock divided by 128 (256 Hz)
11	XO clock divided by 32 (1024 Hz)

### 3.2.8 SYSCFG3

Bit	7	6	5	4	3	2	1	0
<b>0x07</b>	SCLK_SEL_STATUS	XO_CLKOUT_DIV			SPI_AUTO	I2C_PUP_AUTO	I2C_PUP_EN	IO_STR
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	1	1	1	0

Table 23: SYSCFG3 register description

<b>IO_STR</b>	Controls I/O pins' output strength, see 1.9.1 'Digital I/O characteristics'. (0: Normal strength; 1: High strength)
<b>I2C_PUP_EN</b>	Controls internal I <sup>2</sup> C pull-up of $\approx 40\text{K}\Omega$ . (0: Disabled; 1: Enabled)
<b>I2C_PUP_AUTO</b>	I <sup>2</sup> C internal pull-up auto control, requires I2C_PUP_EN to be enabled. (0: Pull-ups always on; 1: Pull-ups in Idle mode disabled)
<b>SPI_AUTO</b>	Controls SPI outputs when its interface is not in use. (0: Always on; 1: Auto disable (HiZ))
<b>XO_CLKOUT_DIV</b>	Enables crystal oscillator and selects division on CLK_OUT pin, see Table 24 'CLK_OUT clock selection'.
<b>SCLK_SEL_STATUS</b>	System clock selection status. (0: Low-power oscillator; 1: Crystal oscillator)

Table 24: CLK\_OUT clock selection

XO_CLKOUT_DIV	Division ratio
000	Disabled
001	Divide by 1 (32 kHz)
010	Divide by 2 (16 kHz)
011	Divide by 4 (8 kHz)
100	Divide by 8 (4 kHz)
101	Divide by 16 (2 kHz)
110	Divide by 32 (1 kHz)

### 3.2.9 TOUT

Bit	7	6	5	4	3	2	1	0
<b>0x08</b>	<b>TOUT_L</b>							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1
Bit	7	6	5	4	3	2	1	0
<b>0x09</b>	<b>TOUT_H</b>							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Table 25: TOUT register description

<b>TOUT_L</b>	Time-out until host wakes up if no wake-up source is triggered, specified as a 16-bit value of system clock periods.
<b>TOUT_H</b>	

### 3.2.10 INTCFG

Bit	7	6	5	4	3	2	1	0
<b>0x0A</b>	<b>PU_S_INT4</b>	<b>PU_INT4</b>	<b>PU_S_INT3</b>	<b>PU_INT3</b>	<b>PU_S_INT2</b>	<b>PU_INT2</b>	<b>PU_S_INT1</b>	<b>PU_INT1</b>
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	1	0	1	0	1

Table 26: INTCFG register description

<b>PU_INT1</b>	
<b>PU_INT2</b>	Enables internal pull-up resistor on interrupt pins.
<b>PU_INT3</b>	(0: Pull-up disabled; 1: Pull-up enabled)
<b>PU_INT4</b>	
<b>PU_S_INT1</b>	
<b>PU_S_INT2</b>	Controls the pull-up resistor strength on the interrupt pins.
<b>PU_S_INT3</b>	(0: Pull-up of $\approx 100k\Omega$ ; 1: Pull-up of $\approx 50k\Omega$ )
<b>PU_S_INT4</b>	

### 3.2.11 CFGP[1-4]

The CFGP[1-4] registers serve the same purpose, affecting peripherals 1 to 4. Only CFGP1 is described below.

Bit	7	6	5	4	3	2	1	0
<b>0x10</b>	<b>INTMOD_P1</b>		<b>PSWMOD_P1</b>		<b>TMOD_P1</b>		<b>PWMOD_P1</b>	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 27: CFGP1 register description

<b>PWMOD_P1</b>	Controls peripheral power mode, see <i>Table 28 'Peripheral power modes'</i> .
<b>TMOD_P1</b>	Controls peripheral polling mode, see <i>Table 29 'Peripheral polling modes'</i> .
<b>PSWMOD_P1</b>	Sets the peripheral power switch mode (pin SW_LP1), see <i>Table 30 'Peripheral power switch mode'</i> .
<b>INTMOD_P1</b>	Sets the peripheral interrupt pin mode (pin INT1), either as an input that can be used during polling, or as a trigger output, see <i>Table 31 'Peripheral interrupt pin mode'</i> .

Table 28: Peripheral power modes

PWMOD_P[1-4]	Power mode
00	Disabled
01	Periodic power-on
10	Invalid
11	Always on

Table 29: Peripheral polling modes

TMOD_P[1-4]	Polling mode
00	Periodic initialization, read data and compare against thresholds
01	Periodic initialization, wait for interrupt, read data and compare against thresholds
10	Periodic initialization and wait for interrupt
11	Wait for an asynchronous interrupt

Table 30: Peripheral power switch mode

PSWMOD_P[1-4]	Pin mode
00	Power switch with output voltage rise detection <b>Warning:</b> do not use this power switch mode as it can cause lock-up when polling. Refer to errata for details.
01	Power switch
10	Logic output (High when peripheral enabled)
11	Logic output inverted (Low when peripheral enabled)

Table 31: Peripheral interrupt pin mode

INTMOD_P[1-4]	Pin mode
00	Interrupt input (active high)
01	Interrupt input (active low)
10	Peripheral trigger output (active high)
11	Peripheral trigger output (active low)

### 3.2.12 MODP[1-4]

The MODP[1-4] registers serve the same purpose, affecting peripherals 1 to 4. Only MODP1 is described below.

Bit	7	6	5	4	3	2	1	0
0x11	SPIMOD_P1		SWPRREG_P1	WUNAK_P1	SEQRW_P1	DTYPE_P1		CMOD_P1
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 32: MODP1 register description

<b>CMOD_P1</b>	Operation trigger area, comparison of <i>over</i> - and <i>under</i> - thresholds, see Figure 14. The default trigger is when the value is equal or higher than the <i>over</i> -threshold or equal or lower than the <i>under</i> -threshold. The inverted trigger is when the value is lower than the <i>over</i> -threshold and higher than the <i>under</i> -threshold. (0: Default trigger; 1: Inverted trigger)
<b>DTYPE_P1</b>	The data type of value read from peripheral, see Table 33 'Peripheral data type configuration'.
<b>SEQRW_P1</b>	Transmit sequential read and write addresses as multi-byte transfers. (0: Disable multi-byte transfers; 1: Enable multi-byte transfers)
<b>WUNAK_P1</b>	Wake up if peripheral does not acknowledge an I <sup>2</sup> C address (NAK). (0: Continue on NAK; 1: Wake up on NAK)
<b>SWPRREG_P1</b>	Swap high/low registers after reading peripheral data. (0: Swap disabled; 1: Swap enabled)
<b>SPIMOD_P1</b>	Sets the SPI mode, see Table 34 'SPI mode configuration'. It requires SPI communication to be enabled via the SPIEN_P1 field in the ADDR_P1 register.

Table 33: Peripheral data type configuration

DTYP_P[1-4]	Data type
00	16-bit unsigned integer
01	16-bit signed integer
10	8-bit unsigned integer
11	Invalid

Table 34: SPI mode configuration

SPIMOD_P[1-4]	SPI mode
00	CPOL: 0, CPHA: 0
01	CPOL: 0, CPHA: 1
10	CPOL: 1, CPHA: 0
11	CPOL: 1, CPHA: 1

### 3.2.13 PERP[1-4]

The PERP[1-4] registers serve the same purpose, affecting peripherals 1 to 4. Only PERP1 is described below.

Bit	7	6	5	4	3	2	1	0
<b>0x12</b>	<b>PERP1_L</b>							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	1	0
Bit	7	6	5	4	3	2	1	0
<b>0x13</b>	<b>PERP1_H</b>							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 35: PERP1 register description

<b>PERP1_L</b>	The polling period for the peripheral is specified as a 16-bit value of system clock periods. This value does not apply if the peripheral power mode is set to disabled or always on.
<b>PERP1_H</b>	<b>NOTE:</b> Zero and one are not valid values and can result in undefined behavior.

### 3.2.14 NCMDP[1-4]

The NCMDP[1-4] registers serve the same purpose, affecting peripherals 1 to 4. Only NCMDP1 is described below.

Bit	7	6	5	4	3	2	1	0
<b>0x14</b>	-	<b>NCMDP1</b>						
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 36: NCMDP1 register description

<b>NCMDP1</b>	Number of write commands for peripheral initialization to be read from SRAM. <b>I<sup>2</sup>C mode:</b> Number of commands to send, where each command consists of an address byte and a value byte. <b>SPI mode:</b> Number of bytes to send from the SRAM for initialization.
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### 3.2.15 ADDR[1-4]

The ADDR[1-4] registers serve the same purpose, affecting peripherals 1 to 4. ADDR1 for peripheral 1 is described below.

Bit	7	6	5	4	3	2	1	0
<b>0x15</b>	<b>SPIEN_P1</b>	<b>ADDR_P1</b>						
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 37: ADDR1 register description

<b>ADDR_P1</b>	<b>I<sup>2</sup>C mode:</b> The 7-bit I <sup>2</sup> C address of the peripheral. <b>SPI mode:</b> Number of bytes to send from SRAM for SPI data read.
<b>SPIEN_P1</b>	Sets which communication protocol should be used with the peripheral. (0: I <sup>2</sup> C; 1: SPI)

### 3.2.16 RREGP[1-4]

The RREGP[1-4] registers serve the same purpose, affecting peripherals 1 to 4. Only RREGP1 is described below.

Bit	7	6	5	4	3	2	1	0
<b>0x16</b>	<b>RREGP1</b>							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 38: RREGP1 register description

<b>RREGP1</b>	Address of the I <sup>2</sup> C peripheral register containing the lower 8 bits of the value to be read. When the data type is 16-bit, this register is incremented to retrieve the higher 8 bits.
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### 3.2.17 THROVP[1-4]

The THROVP[1-4] registers serve the same purpose, affecting peripherals 1 to 4. Only THROVP1 is described below.

Bit	7	6	5	4	3	2	1	0
<b>0x17</b>	<b>THROVP1_L</b>							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
<b>0x18</b>	<b>THROVP1_H</b>							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 39: THROVP1 register description

<b>THROVP1_L</b> <b>THROVP1_H</b>	The value of the peripheral <i>over</i> -threshold, up to 16-bit, should match the data type set in DTYPE_P1 (see Table 33 'Peripheral data type configuration').
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### 3.2.18 THRUNP[1-4]

The THRUNP[1-4] registers serve the same purpose, affecting peripherals 1 to 4. Only THRUNP1 is described below.

Bit	7	6	5	4	3	2	1	0
<b>0x19</b>	<b>THRUNP1_L</b>							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
<b>0x1A</b>	<b>THRUNP1_H</b>							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 40: THRUNP1 register description

<b>THRUNP1_L</b> <b>THRUNP1_H</b>	The value of the peripheral <i>under</i> -threshold, up to 16-bit, should match the data type set in DTYPE_P1 (see Table 33 'Peripheral data type configuration').
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### 3.2.19 TWTP[1-4]

The TWTP[1-4] registers serve the same purpose, affecting peripherals 1 to 4. Only TWTP1 is described below.

Bit	7	6	5	4	3	2	1	0
<b>0x1B</b>	<b>TWTP1</b>							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 41: TWTP1 register description

<b>TWTP1</b>	The period of time to wait before and/or after peripheral initialization until the value is read, or until timeout while waiting for an interrupt assertion, defined in units of 256 or 4096 periods of the internal 400 kHz oscillator. The actual time to wait and when to wait, depends on the value of the TCFGP1 register fields.
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### 3.2.20 TCFGP[1-4]

The TCFGP[1-4] registers serve the same purpose, affecting peripherals 1 to 4. Only TCFGP1 is described below.

Bit	7	6	5	4	3	2	1	0
<b>0x1C</b>	-	<b>I2CRET_P1</b>		<b>TINIT_EXT_P1</b>	<b>TINIT_EN_P1</b>	<b>TWT_EXT_P1</b>	<b>TWT_EN_P1</b>	
Type	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 42: TCFGP1 register description

<b>TWT_EN_P1</b>	Enable post-initialization wait time, as defined by TWTP1.
<b>TWT_EXT_P1</b>	Extends the post-initialization wait time to be TWTP1 units of 4096 periods of the internal 400 kHz oscillator, instead of the default 256. (0: Pre-init time x256 clocks; 1: Pre-init time x4096 clocks)
<b>TINIT_EN_P1</b>	Enable pre-initialization wait time, as defined by TWTP1.
<b>TINIT_EXT_P1</b>	Extends the pre-initialization wait time to be TWTP1 units of 4096 periods of the internal 400 kHz oscillator, instead of the default 256. (0: Post-init time x256 clocks; 1: Post-init time x4096 clocks)
<b>I2CRET_P1</b>	The number of I <sup>2</sup> C peripheral communication retries in case of NAK. A value of 0 means no retries, the polling is aborted immediately when a NAK is received.

### 3.2.21 THROVA1

Bit	7	6	5	4	3	2	1	0
0x44	-			THROVA1				
Type	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 43: THROVA1 register description

<b>THROVA1</b>	The value of the internal ADC channel <i>over</i> -threshold, defined as 5-bit unsigned.
----------------	--

### 3.2.22 THRUNA1

Bit	7	6	5	4	3	2	1	0
0x45	-			THRUNA1				
Type	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 44: THRUNA1 register description

<b>THRUNA1</b>	The value of the internal ADC channel <i>under</i> -threshold, defined as 5-bit unsigned.
----------------	---

### 3.2.23 THROVA2

Bit	7	6	5	4	3	2	1	0
0x46	-		THROVA2					
Type	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 45: THROVA2 register description

<b>THROVA2</b>	The value of the external ADC channel <i>over</i> -threshold, defined as 6-bit unsigned.
----------------	--

### 3.2.24 THRUNA2

Bit	7	6	5	4	3	2	1	0
0x47	-		THRUNA2					
Type	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Table 46: THRUNA2 register description

<b>THRUNA2</b>	The value of the external ADC channel <i>under</i> -threshold, defined as 6-bit unsigned.
----------------	---

### 3.2.25 VALP[1-4]

The VALP[1-4] registers serve the same purpose, affecting peripherals 1 to 4. Only VALP1 is described below.

Bit	7	6	5	4	3	2	1	0
<b>0x50</b>	<b>VALP1_L</b>							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
<b>0x51</b>	<b>VALP1_H</b>							
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Table 47: VALP1 register description

<b>VALP1_L</b> <b>VALP1_H</b>	The last read value from peripheral, either 8-bit or 16-bit, matching the data type set in DTYPE_P1. (see <i>Table 33 'Peripheral data type configuration'</i> )
----------------------------------	---

### 3.2.26 ADC\_CORE

Bit	7	6	5	4	3	2	1	0
<b>0x58</b>	-			<b>ADC_CORE</b>				
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	X	X	X	X	X

Table 48: ADC\_CORE register description

<b>ADC_CORE</b>	The last read value from the internal ADC channel (VBAT pin), see <i>Table 50 'ADC codes'</i> .
-----------------	---

### 3.2.27 ADC\_EXT

Bit	7	6	5	4	3	2	1	0
0x59	-		ADC_EXT					
Type	R	R	R	R	R	R	R	R
Reset	0	0	X	X	X	X	X	x

Table 49: ADC\_EXT register description

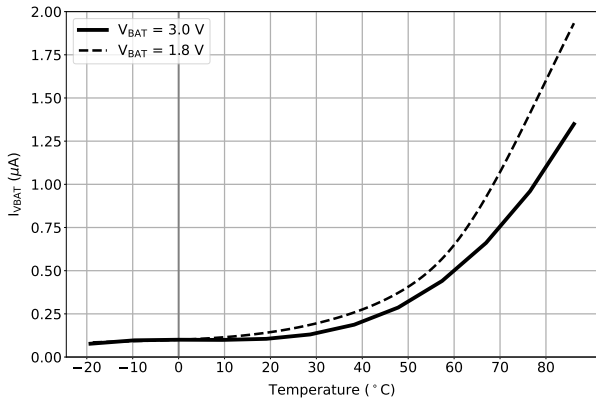
<b>ADC_EXT</b>	The last read value from the external ADC channel (ADC_IN pin), see <i>Table 50 'ADC codes'</i> .
----------------	---

Table 50: ADC codes

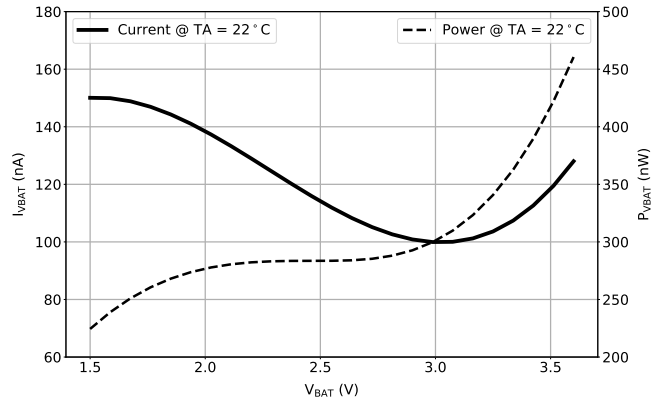
In (V)	ADC_EXT	ADC_CORE	In (V)	ADC_EXT	ADC_CORE
0.6	0x00	-	2.1	0x2C	0x0C
0.7	0x08	-	2.2	0x2D	0x0D
0.8	0x0F	-	2.3	0x2E	0x0E
0.9	0x15	-	2.4	0x2F	0x0F
1.0	0x19	-	2.5	0x2F	0x0F
1.1	0x1C	-	2.6	0x30	0x10
1.2	0x1F	-	2.7	0x31	0x11
1.3	0x22	-	2.8	0x31	0x11
1.4	0x23	-	2.9	0x32	0x12
1.5	0x24	0x04	3.0	0x32	0x12
1.6	0x26	0x06	3.1	0x33	0x13
1.7	0x28	0x08	3.2	0x33	0x13
1.8	0x29	0x09	3.3	0x33	0x13
1.9	0x2A	0x0A	3.4	0x34	0x14
2.0	0x2B	0x0B	3.6	0x34	0x14

## 4 Typical performance

In this section, graphs are provided to illustrate the typical behavior of the nPZero IC, including Standby and Idle current values under different temperature and supply voltage conditions, host switch ON resistance, and ADC curves.

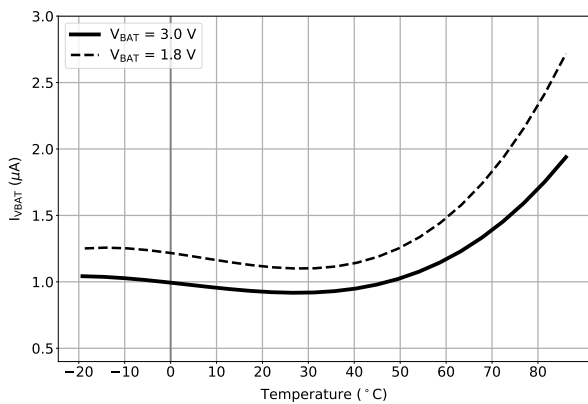


(a) VBAT current vs Temperature in Idle mode

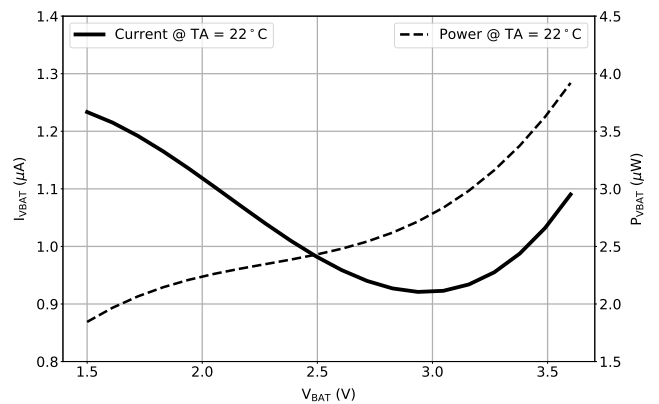


(b) VBAT current and power vs VBAT in Idle mode

Figure 21: Typical performance in Idle mode

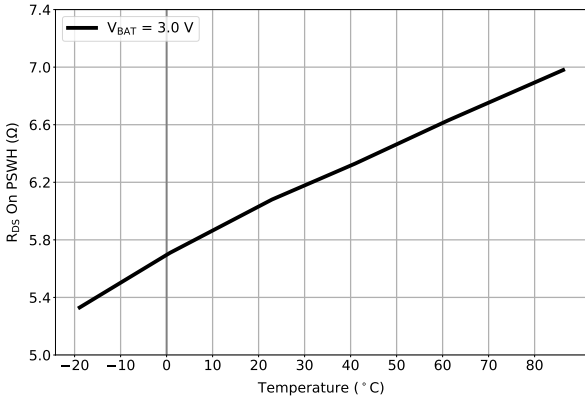


(a) VBAT current vs Temperature in Standby mode

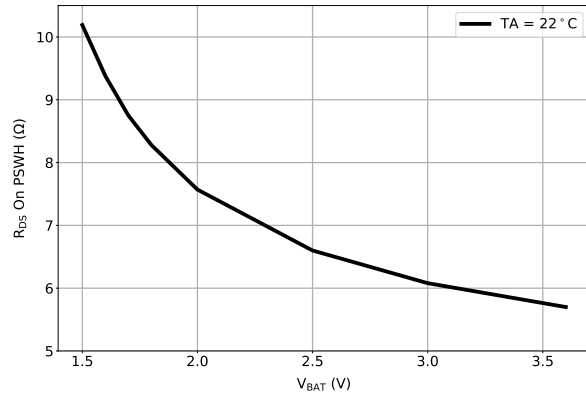


(b) VBAT current and power vs VBAT in Standby mode

Figure 22: Typical performance in Standby mode

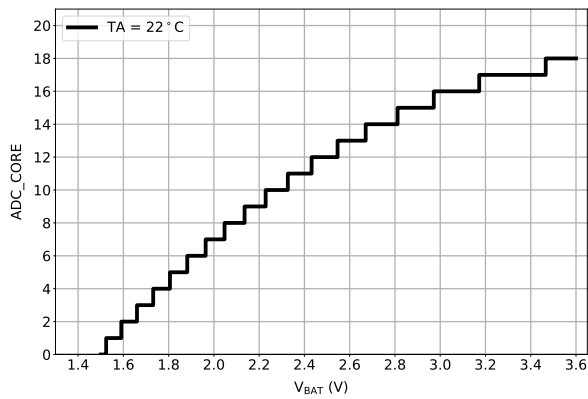


(a) Host Switch ON Resistance vs Temperature

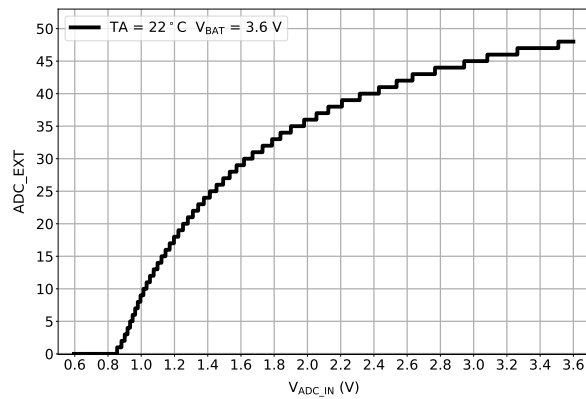


(b) Host Switch On Resistance vs VBAT

Figure 23: Typical Host Switch ON Resistance



(a) Curve for ADC\_CORE vs VBAT



(b) Curve for ADC\_EXT vs ADC\_IN

Figure 24: Typical ADC curves

## 5 Mechanical Specifications

### 5.1 QFN32 Package

5.00 mm × 5.00 mm body, 0.80 mm height (max), 0.50 mm pitch

#### 5.1.1 Outline Drawing

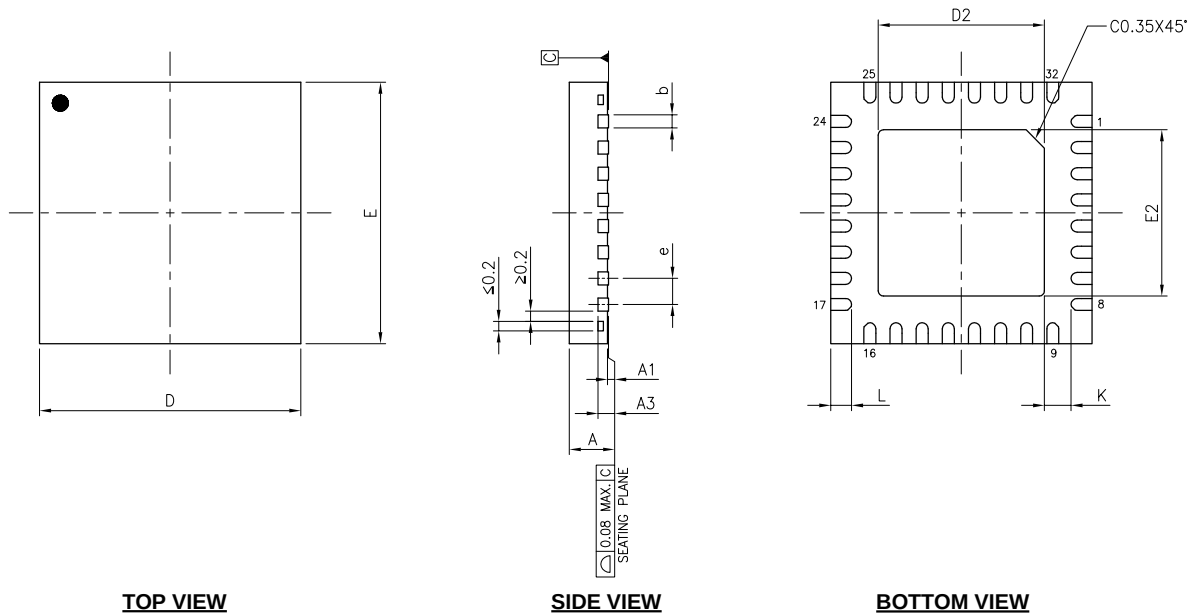


Figure 25: QFN32 packaging outline

Table 51: QFN32 packaging dimensions

Symbol	A	A1	A3	b	D/E	e	L	K	D2	E2
Dimension (mm)	Min.	0.70	0.00	0.203 REF	0.18	5.00 BSC	0.35	0.20	3.15	3.15
	Nom.	0.75	0.02		0.25		0.40	–	3.20	3.20
	Max.	0.80	0.05		0.30		0.45	–	3.25	3.25

#### Notes:

- All dimensions are in millimeters.
- Dimension **b** applies to the metalized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension **b** should not be measured in that radius area.
- A bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.
- Drawing confirms to JEDEC MO-220, variation W(V)HHD-2.

### 5.1.2 Land Pattern

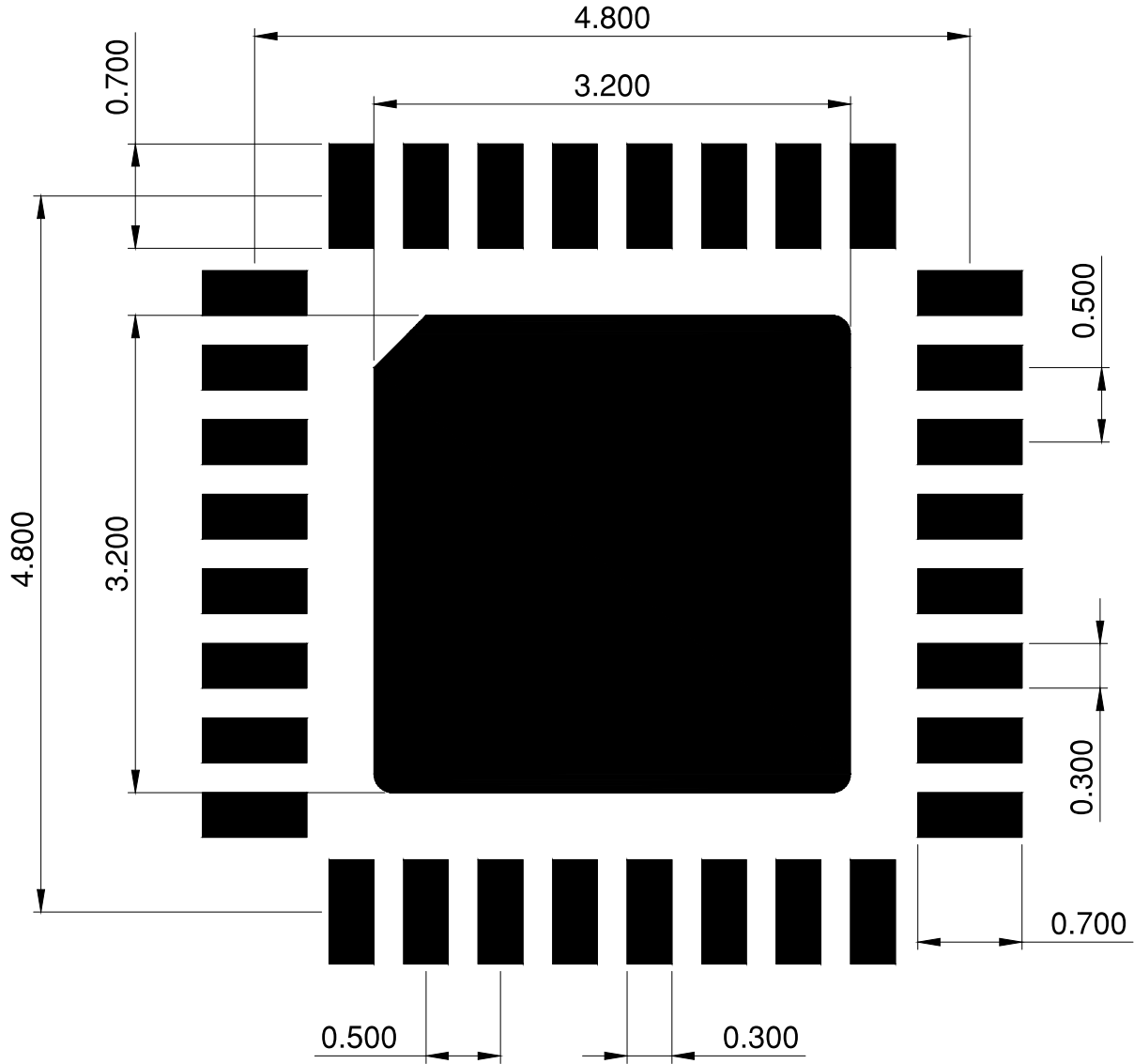


Figure 26: QFN32 package land pattern

**Notes:**

1. All dimensions are in millimeters.

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